SHIVAJI UNIVERSITY
M.TECH (Electronics Technology) PROGRAMMES

Course Structure and Scheme of Evaluation
Semester I

Course Code	Course	Teaching Scheme			
		L	T	P	Credits
C 10	Research Methodology (Audit)	2	-	-	-
C11	High Speed Analog Design	4	-	-	4
C12	Reconfigurable Platforms & HDL	4	-	-	4
C 13	Communication Networks	4	-	-	4
E 14	Elective-I	3	-	-	3
E 15	Elective-II	3	-	-	3
C 14	High Speed Analog Design Lab	-	-	2	1
C 15	Reconfigurable Platforms & HDL Lab	-	-	2	1
C 16	Communication Networks Lab	-	-	2	1
S 16	Seminar –I	-	-	2	2
	Total	**20**	**0**	**8**	**23**
	Total Contact hours per week = 28				

Elective - I

E14(V) Memory Technologies

E 14 (V) CMOS VLSI Design

E14(E) Asynchronous Circuit Design

E 14 (E) Advanced Computer Architecture

Elective - II

E15(V) Digital System And Testing

E 15 (V)Mixed Signal ASIC Design

E 15 (E) RISC Microcontrollers

E 15 (E) Automotive Embedded Systems

Specialization : V VLSI Design
E Embedded Systems

SHIVAJI UNIVERSITY
M.TECH (Electronics Technology) PROGRAMMES

Course Structrue and Scheme of Evaluation
Semester II

Course Code	Course	Teaching Scheme			
		L	T	P	Credits
C 21	DSP Processor	4	-	-	4
C 22	Real Time Operating System	4	-	-	4
C 23	High Speed Digital Design	4	-	-	4
E 24	Elective-III	3	-	-	3
E 25	Elective-IV	3	-	-	3
C 24	DSP Processor Lab	-	-	2	1
C 25	Real Time Operating System Lab	-	-	2	1
C 26	High Speed Digital Design Lab	-	-	2	1
S 26	Seminar –II	-	-	2	2
	Total	**18**	**0**	**8**	**23**
	Total Contact hours per week = 26				

Elective – III

E24(V) System on Chip

E 24 (V) Wavelet Transform and Applications
E24(E) MicroElctroMechanical System

E 24 (E) Robotics and Machine Vision

Elective - IV

E25(V) RF Integrated Circuit Design

E 25 (V) VLSI in Signal Processing
E25(E) High Performance Networks

E 25 (E) Mobile Computing

Specialization : V VLSI Design
E Embedded Sysems

SHIVAJI UNIVERSITY
M.TECH (Electronics Technology) PROGRAMMES

Course Structrue and Scheme of Evaluation
Semester III

Course Code	Course	Teaching Scheme			
		L	T	P	Credits
T 31	* Industrial Training	-	-	**2	4
S 32	Dissertation Phase-I	-	-	**5	10
	Total	**-**	**-**	**7**	**14**
	**Total Contact hours per week/students = 2 &5 respectively for T31 & S32				

8 Weeks at the end of First Year (Summer)
** Average contact hours/week/student

Course Structure and Scheme of Evaluation
Semester IV

Course Code	Course	Teaching Scheme			
		L	T	P	Credits
D 42	Dissertation Phase-II	-	-	5	20
	Total	**-**	**-**	**5**	**20**
	Total Contact hours per week = 5				

Semester I

C-10 Research Methodology

Teaching SchemeExamination Scheme
Lectures: 2 Hrs./Week

Unit 1 Research Methodology: An Introduction **4hrs.**

Objectives of Research, Types of Research, Research Methods and Methodology, Defining a Research Problem, Techniques involved in Defining a Problem

Unit 2 Research Design **6hrs.**

Need for Research Design, Features of Good Design, Different Research Designs, Basic Principles of Experimental Designs, Sampling Design, Steps In Sampling Design, Types of Sampling Design, Sampling Fundamentals, Estimation, Sample size Determination, Random sampling

Unit 3 Measurement and Scaling Techniques **4hrs.**

Measurement in Research, Measurement Scales, Scales, Sources in Error, Techniques of Developing Measurement Tools, Scaling, Meaning of Scale, Scale Construction Techniques

Unit 4 Methods of Data Collection and Analysis **4hrs.**

Collection of Primary and Secondary Data, Selection of appropriate method, Data Processing Operations, Elements of Analysis, Statistics in Research, Measures of Dispersion, Measures of Skewness, Regression Analysis, Correlation

Unit 5 Techniques of Hypotheses, Parametric or Standard Tests **4hrs.**

Basic concepts, Tests for Hypotheses I and II, Important parameters, Limitations of the tests of Hypotheses, Chi-square Test, Comparing Variance, as a non-parametric Test, Conversion of Chi to Phi, Caution in Using Chi- square test

Unit 6Analysis of Variance and Co-variance **4hrs.**

ANOVA, One way ANOVA, Two Way ANOVA, ANOCOVA, Assumptions in ANOCOVA, Multivariate Analysis Technique, Classification of Multivariate Analysis, factor Analysis, R-type Q Type Factor Analysis, Path Analysis

Interpretation and Report **1hrs.**

SHIVAJI UNIVERSITY
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Semester I

C 11 High Speed Analog Design Techniques

Teaching SchemeExamination Scheme
Lectures: 4 Hrs./Week
Credit: 4
Practical: 2Hrs/Week
Credit: 1

Unit 1: High Speed Operational Amplifiers **6hrs.**

Folded Cascode Voltage Feedback Op-Amps, Case study of AD847, Current Feedback Op-Amps (CFB), CFB model and Bode plot, study of AD8011, Comparison of specifications of Current feedback Op-amp family AD8001, AD8002, AD8009 and AD8073, Noise comparisons between VFB and CFB Op Amps, PSRR Characteristics. **7hrs.**

Unit 2: High-Speed applications based on Op-amps

Optimizing feedback network for maximum bandwidth fitness, Driving Capacitive load, Cable drivers and receivers, High performance video line driver, Differential line drivers and receivers, High speed clamping amplifiers, High speed current to voltage converters and the effects of inverting input capacitance, **6hrs.**

Unit 3: High speed amplifiers for communication applications

Low noise amplifiers for communication systems, Mixers, Power amplifiers, Liner drivers, Automatic gain control amplifiers **7hrs.**

Unit 4: High speed system for video applications

High speed video multiplexing with Opamps using disable function, Video programmable gain amplifier, Video multiplexers and Cross Point switches, High power line drivers and ADSL, High speed photodiode Pre amps, Case studies of AD830, AD9002 **6hrs.**

Unit 5: High speed RF/IF Subsystems

Dynamic range compression, Linear VCAs, Log/Limiting Amplifiers, Receiver overview, Multipliers, modulators and mixers, **7hrs.**

Unit 6:

Case study of AD600 Dual Channel X-amp, AD641 monolithic log amplifier.

Reference Books:

1. Intuitive Operational Amplifiers, Thomas M. Frederiksen, McGraw Hill, 1988.
2. B Razavi, "RF Microelectronics", Prentice Hall, 1998
3. T.H. Lee, "The Design of CMOS Radio-Frequency Integrated Circuits" Cambridge University Press, 1998.
4. High Speed Design Techniques, Manual by analog Devices, October 1996
5. Modular Low-Power, High Speed CMOS Analog-to-Digital Converter for Embedded Systems, Lin, Dr. Ing.Keh-La Kemma, Armin Hosticka, Prof. Bedrich J. Publisher, Kluwer Academic Publishers

SHIVAJI UNIVERSITY
M.TECH (Electronics Technology) PROGRAMMES

Semester I

C 12 Reconfigurable Platforms and HDL

Teaching SchemeExamination Scheme
Lectures: 4 Hrs./Week
Credit: 4
Practical:2Hrs/week
Credit: 1

Unit 1:
Computing requirements, Area, Technology scaling, Instructions,Custom ComputingMachine, Overview, Comparison of Computing Machines. **6hrs.**

Unit 2:
Interconnects, Requirements, Delays in VLSI Structures; Partitioning and Placement, Routing; Computing Elements, LUT's, LUT Mapping, **7hrs.**
ALU and CLB's, Retiming, Fine-grained & Coarse-grained structures; Multicontext; Comparison of different architectures viz. PDSPs, RALU, VLIW, Vector Processors, Memories,

Unit 3:
Arrays for fast computations, CPLDs, FPGAs, Multicontext, Partial Reconfigurable Devices; **6hrs.**
TSFPGA, DPGA, Mattrix; Best suitable approach for RD; Case study. Control Logic, Binding Time and Programming Styles, Overheads, Data Density, Data BW, Function density, Function diversity, Interconnect methods, Best suitable methods for RD;

Unit 4:
Contexts, Context switching; Area calculations for PE;Efficiency, ISP, Hot Reconfiguration; **7hrs.**
Case study. Architectures for existing multi FPGA systems, Compilation Techniques for mapping applications described in a HDL to reconfigurable hardware, Study of existing reconfigurable computing systems to identify existing system limitations and to highlight opportunities for research;

Unit 5:
Software challenges in System on chip; Testability challenges; Case studies. Modeling, **6hrs.**
Temporal portioning algorithms, Online temporal placement, Device space management,

Unit 6:
Direct communication, Third party communication, Bus based communication, Circuit **7hrs.**
switching, Network on chip, Dynamic network on chip, Partial reconfigurable design.

References:

1. Andre Dehon, "Reconfigurable Architectures for General Purpose Computing".
2. IEEE Journal papers on Reconfigurable Architectures.
3. "High Performance Computing Architectures" (HPCA) Society papers.
4. Christophe Bobda, "Introduction to Reconfigurable Computing", Springer Publication.
5. Maya Gokhale, Paul Ghaham, "Reconfigurable Computing", Springer Publication.

SHIVAJI UNIVERSITY

M.TECH (Electronics Technology) PROGRAMMES

Semester I

C 13 Communication Networks

Teaching SchemeExamination Scheme
Lectures: 4 Hrs./Week
Credit: 4
Practical: 2Hrs/Week
Credit: 1

6hrs.

Unit:1 Ipv6 Networks

Advanced IPv6 features, including transition. Mobile IPv6 operation. Models to support (WLAN) network roaming , IPv6 transition methods ;

7hrs.

Unit 2: Network Security

Advanced IP routing and multihoming, Challenging networking scenarios.Advanced security issues ' Network performance and monitoring. Advanced IP Multicast

6hrs.

Unit 3: Configuring the Network:

Link-local and Adminstrator-less networking.Topics in Dynamic Host Configuration, Node and Service Discovery, Multi-homing in Enterprise networks. Issues with renumbering live networks

7hrs.

Unit 4: TCP/IP and Wireless communication technologies:

TCP/IP fundamentals, Reviews on wireless communication technologies, WLAN, Bluetooth, TCP/IP over Wireless Networks

Unit 5: P2P and Overlay Network:

Routing, Multicast, Content Distribution Networks, Content addressing, search, and retrieval

Unit 6: Different type of advanced networks

6hrs.

Bluetooth, 802.11. HiperLAN2, GPRS and Edge Services, UMTS, 3G, Beyond 3G: integrated 4G services. Access technologies: last mile, xDSL, Reviews of packet switching, Advanced topics in Computer Networking Multimedia over a Network, Streaming over Internet, Streaming over wired and wireless Network, Wireless Sensor Networks, Wireless Home Networks

Reference Books

1. Computer Networking: A Top-Down Approach Featuring the Internet, by James Kwose and Keith Ross, ISBN: 0-201-97699-4, Addison-Wesley, 2/e, 2002
2. IP SANS: A Guide to iSCSI, iFCP, and FCIP Protocols for Storage Area Networks, by Thomas dark, ISBN: 0-201-75277-8, Addison-Wesley, 2002
3. Storage Area Network Fundamentals, by Meeta Gupta, ISBN: I-58705-065-X, Prentice Hall, April 2002 ^ ;;.-
4. Designing Storage Area Networks: A Practical Reference for Implementing Fibre Channel and IP SANs, 2/E, by Tom dark, ISBN: 0-321-13650-0, Addison-Wesley, 2003
5. Wireless Communications and Networks, by William Stallings, ISBN: 0-13-040864-6, Prentice Hall, 2002
6. Computer Networks: A Systems Approach, 2/e, by Lan-y Peterson and Bruce Davie, ISBN: 1-55860-514-2, Morgan Kaufinann Publishers, 2000

Semester I

C 14 High Speed Analog Design Lab

Pratical : 2 hrs./week **Credit :** 1

Students are instructed to frame and perform laboratory assignments, based on each of theory course. The assignment should encompass the hardware techniques and software tools introduced in the concerned subjects and should prove to be useful for the PG programs in the relevant discipline. Assignment should be a full-fledged system design type problem with multi-dimensional solutions suggested. Assignment should be implemented using known hardware techniques/software tools and should be reliably executable.

Student shall submit a laboratory work document based on these assignments performed at the end of semester. The Laboratory instructor shall guide the students in framing the assignments and defining the problem pertaining to the said subjects.

C 15 Reconfigurable Platforms & HDL Lab

Pratical : 2 hrs./week **Credit :** 1

Students are instructed to frame and perform laboratory assignments, based on each of theory course. The assignment should encompass the hardware techniques and software tools introduced in the concerned subjects and should prove to be useful for the PG programs in the relevant discipline. Assignment should be a full-fledged system design type problem with multi-dimensional solutions suggested. Assignment should be implemented using known hardware techniques/software tools and should be reliably executable.

Student shall submit a laboratory work document based on these assignments performed at the end of semester. The Laboratory instructor shall guide the students in framing the assignments and defining the problem pertaining to the said subjects.

SHIVAJI UNIVERSITY

M.TECH (Electronics Technology) PROGRAMMES

Semester I

C 16 Communication Network Lab

Pratical : 2 hrs./week **Credit :** 1

Students are instructed to frame and perform laboratory assignments, based on each of theory course. The assignment should encompass the hardware techniques and software tools introduced in the concerned subjects and should prove to be useful for the PG programs in the relevant discipline. Assignment should be a full-fledged system design type problem with multi-dimensional solutions suggested. Assignment should be implemented using known hardware techniques/software tools and should be reliably executable.

Student shall submit a laboratory work document based on these assignments performed at the end of semester. The Laboratory instructor shall guide the students in framing the assignments and defining the problem pertaining to the said subjects.

SHIVAJI UNIVERSITY
M.TECH (Electronics Technology) PROGRAMMES

Semester I

ELECTIVE-I

E14 (V) Memory Technologies

Teaching SchemeExamination Scheme
Lectures: 3 Hrs./Week
Credit: 3

Unit 1
Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, SOl, Advanced SRAM Architectures, Application Specific SRAMs; **6hrs.**

Unit 2
DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAM, **7hrs.**

Unit 3
High Density ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Nonvolatile SRAM, Flash Memories. RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory **6hrs.**

Unit 4
Testing.General Reliability Issues, RAM Failure Modes and Mechanism, Nonvolatile Memory, Reliability Modeling and Failure Rate Prediction, Reliability Screening and Qualification. Radiation Effects, SEP,Radiation Hardening Techniques. **7hrs.**

Unit 5
Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing, Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices. **6hrs.**

Unit 6
Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging, Future Directions, Introduction to digital tablet PC, LCD, DVD player etc. **7hrs.**

References:
1. Ashok K.Sharma, " Semiconductor Memories Technology, Testing and Reliability ",Prentice-Hall of India Private Limited, New Delhi, 1997.
2. Memories", Springer Publication.
3. Wen C. Lin, "Handbook of Digital System Design", CRC Press.

SHIVAJI UNIVERSITY
M.TECH (Electronics Technology) PROGRAMMES

Semester I

E14 (V) CMOS VLSI Design

Teaching SchemeExamination Scheme
Lectures: 3 Hrs./Week
Credit: 3

Unit 1: Basics of CMOS

VLSI Design: History, Trends, Principles, Metrics, CMOS transistors (n-channel and p-channel), The CMOS Switch model, CMOS Inverter mode, Logic devices and interconnect, CMOS circuit analysis: transistors, inverters, interconnect modeling, parasitics, CMOS Process and Layout, CMOS Devices: SPICE and deep sub-micron issues **6hrs.**

Unit 2: CMOS: Design Issues

CMOS Inverter: speed, power and scaling, Static CMOS Gates, Dynamic CMOS Gates, Power Estimation and Optimization **7hrs.**

Unit 3: Modeling

Analytical modeling: Ellmore Delay, Transmission models, RC, RLC lumped parameter models, Layout for custom logic: Sea of Gates (SoG) model, Design rules, Circuit fabrication methods for CMOS, Levels of abstraction. **6hrs.**

Unit 4: Circuits to Systems

VLSI circuits to systems, Circuit modeling and layout (demo using standard tools), CMOS design and layout tools, Nano-electronics circuits versus CMOS microelectronics circuits, Nano-computing techniques and device platforms **7hrs.**

Unit 5: Digital IC Design

Digital CMOS IC design: Sequential Logic Circuits, Implementation Strategies for Digital ICs, Interconnects, Timing and Clocking, Datapath Design, Memory Design, Capactitiveparasitics, Resistive parasitics, Inductive parasitics **6hrs.**

Unit 6: Timing issues for Digital CMOS circuits

Timing Issues, Clock skew, clocking styles, Self-timed circuit design, Case study of Kitchen timer chip **7hrs.**

Reference Books:

1. N.H.E. Weste and K. Eshraghian, "Principles of CMOS VLSI Design", New Uork: Addison-Wesley, 1993.
2. Christopher Saint and Judy Saint, "IC Layout Basics", McGraw Hill Publications
3. Weste and Harris, CMOS VLSI Design, a Circuits and Systems Perspective (3 rd edition)
4. by Jan M. Rabaey, A. Chandrakasan, B. Nikolic, Digital Integrated Circuits (2nd Edition) Prentice Hall, 2003.

SHIVAJI UNIVERSITY
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Semester I

E 14 (E) Asynchronous Circuit Design

Teaching SchemeExamination Scheme
Lectures: 3 Hrs./Week
Credit: 3

Unit 1. **6hrs.**
Introduction to asynchronous circuit design, Communication channels, Modeling asychronous communication in VHDL,Example: MiniMIPS

Unit 2.
Communication protocols, Handshaking expansion, Data Encoding, Syntax-directed translation, Graphical representations, Asynchronous finite state machines, Petri nets,Timed event/level structures **7hrs.**

Unit 3 **6hrs.**
Huffman circuits, Solving covering problems, State minimization, State assignment, Hazard-free logic synthesis, Extensions for MIC operation

Unit 4. **7hrs.**
Muller circuits, Complete state coding Hazard-free logic synthesis, Hazard-free ,decomposition

Unit 5
Timing circuits, Zones, POSET Timing,Verification , Circuit verification ,Protocal verification **6hrs.**

Unit 6.
Applications , History/RAPPID , Performance analysis/testing , Synchronization problem **7hrs.**

References Book:

"Asynchronous Circuit Design", Chris J. Myers, John Wiley & Sons, Inc

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Semester I

E 14 (E) Advanced Computer Architecture

Teaching SchemeExamination Scheme
Lectures: 3 Hrs./Week
Credit: 3 .

UNIT 1 INSTRUCTION LEVEL PARALLELISM **6hrs.**
ILP – Concepts and challenges – Hardware and software approaches – Dynamic scheduling – Speculation - Compiler techniques for exposing ILP – Branch prediction.

UNIT 2 MULTIPLE ISSUE PROCESSORS
VLIW & EPIC – Advanced compiler support – Hardware support for exposing parallelism – Hardware versus software speculation mechanisms – IA 64 and Itanium processors – Limits on ILP. **7hrs.**

UNIT 3 MULTIPROCESSORS AND THREAD LEVEL PARALLELISM **6hrs.**
Symmetric and distributed shared memory architectures – Performance issues – Synchronization – Models of memory consistency – Introduction to Multithreading.

UNIT 4 MEMORY AND I/O
Cache performance – Reducing cache miss penalty and miss rate – Reducing hit time – Main memory and performance – Memory technology. Types of storage devices – Buses – RAID – Reliability, availability and dependability – I/O performance measures – Designing an I/O system. **7hrs.**

UNIT 5 MULTI-CORE ARCHITECTURES **6hrs.**
Software and hardware multithreading – SMT and CMP architectures – Design issues –

UNIT 6 Case studies – Intel Multi-core architecture – SUN CMP architecture - heterogenous multi-core processors – case study: IBM Cell Processor. **7hrs.**

TEXT BOOKS:

1. John L. Hennessey and David A. Patterson, " Computer architecture – A quantitative approach", Morgan Kaufmann / Elsevier Publishers, 4th. edition, 2007.

REFERENCES:

1. David E. Culler, Jaswinder Pal Singh, "Parallel computing architecture: A hardware/software approach" , Morgan Kaufmann /Elsevier Publishers, 1999.
2. Kai Hwang and Zhi.WeiXu, "Scalable Parallel Computing", Tata McGraw Hill, New Delhi, 2003.

SHIVAJI UNIVERSITY

M.TECH (Electronics Technology) PROGRAMMES

Semester I

Elective –II

E 15 (V) Digital Systems and Testing

Teaching SchemeExamination Scheme
Lectures: 3 Hrs./Week
Credit: 3

Unit 1: Testing **6hrs.**

Testing Defined: definitions and areas within testing. Logic and Fault Modeling. Mechanics

Definitions: Abstractions level, Faults and errors , Modeling, Test Evaluation, Test Generation, Diagnostics.

Unit 2:System life, Sources of defects?

Representation and models of digital systems across abstraction levels. **7hrs.**

Fault Models: logical versus physical; SSL model, opens and shorts, bridging faults; Basic assumptions.
Review of minimization tools and asynchronous machines, Test Pattern Generation basics. (activate and drive.), Algebraic approaches, Fault Equivalence and Dominance.

Unit 3:Test Generation **6hrs.**

Algebraic Approaches and Structural Approaches, Logic Simulation.

Algebraic Approaches: Boolean difference, Literal position, Effect of fanout on circuits, Checkpoint faults.

Structural Approaches to test generation. Path sensitization methods. Test Coverage

Unit 4:Logic simulations **7hrs.**

Simulation engines: compiler, event driven. Representation of value, circuit, etc.

Logic and Fault Simulation: Delay models for circuit simulation, Fault Simulation Purpose of Serial and Parallel Fault Simulation, Deductive fault simulation. Concurrent Fault Simulation, Critical Path tracing, Statistical Fault Analysis

Unit 5:More Test Generation and D-algorithm

D-algorithm.representation, cube algebra, generalized algorithm, Extensions to D-algorithm PODEM, FAN, etc. Random test generation, Complexity issues Functional Test Generation Methods, Heuristic Methods, Exhaustive and Pseudo Exhaustive techniques, RAM and PLA testing, Microprocessor testing, Memory Testing: Memory test complexity, Memory fault models. **6hrs.**

Unit 6: Design for Testability **7hrs.**

Controllability and Observabilitymeasures.STEFAN, Ad Hoc techniques, More Design for Testability, Scan Design.Scan Designs: IEEE Standards, Board-Level Testing: Boundary Scan, Data Compression and BIST, LFSR polynomial generation Data compression techniquesAliasing Probability, BIST, Self Checking and PLD Testing

References:

1. "Digital Systems Testing and Testable Design" by MironAbramovici, Melvin Breuer and Arthur Friedman, IEEE press, NY.
2. A Guide to VHDL" by Stanley Mazor, Kluwer Academic Press
3. "HDL Chip Design" by Douglas Smith, Doone Publications, AL.
4. "Rapid Prototyping of Digital Systems", by J. O. Hamblen and M. Furman, Kluwer Academic Publishers.

SHIVAJI UNIVERSITY

M.TECH (Electronics Technology) PROGRAMMES

Semester I

E 15 (V) Mixed Signal ASIC Design

Teaching SchemeExamination Scheme
Lectures: 3 Hrs./Week
Credit: 3

Unit 1: Technology and modeling aspects of an advanced BiCMOS ASIC process **6hrs.**

LSI Logic analogue BiMOS technology, Background, Process technology, Well formation, Island definition and field region implants, Field oxidation - Island formation, High performance operational amplifiers and comparators

High performance amplifiers, The load compensated OTA (LC-OTA), The Miller compensated OTA (M-OTA), The core-amplifier (C-OTA), High performance comparators, The OTA as comparator, Latched comparators, A high speed accurate comparator.

Unit 2: Switched current techniques for analogue sampled data signal processing **7hrs.**

Introduction, First generation memory cells, Second generation memory cells, Limitations of the basic SI memory cell, Channel length modulation, Charge injection, Junction leakage Applications: Integrator based biquad, FIR filters, Sigma-Delta modulators

Unit 3: Data converters

Parameters for data converter characterisation, Data converters: Basic design considerations, High speed data conversion techniques, Current switched D/A converters, Flash and two-step flash converters, Limits to speed and resolution in data converters Oversampling converters, Intuitive Introduction to Oversampling Data Converters, Noise shaping converters, First order sigma delta modulators Second order sigma delta modulator, Multistage sigma-delta modulator, Non ideal effects in sigma delta modulators, Sampling jitter **6hrs.**

Unit 4: Self-callibrating and algorithmic converters **7hrs.**

Self-calibrated analogue-digital converters, Architecture with segmented binary-weighted capacitor Array, Self-calibration technique and circuits, Principle of calibration, Calibrating capacitors, Calibrating registers

Unit 5: A high flexibility BiCMOS standard cell library for mixed analogue-digital ASICs **6hrs.**

A BiCMOS process dedicated to mixed A/D applications, Cell libraries, Analogue libraries, The digital cell library, CAD tools, The CAD capability, Telescopic Cells, Parametrizable cells, Adjustable cells, Automatic cell biasing and power down, ADS (Analog Design System) An environment for Mixed signal design, Analogue/digital multi-level mixed mode simulations, Case Studies:

Example 1: Infra red receiver with decoder and actuator Example 2: Remote control

Unit 6: Advanced topics: **7hrs.**

Element matching, Local process variations, Global process variations, Process gradients, Boundary effects, Noise coupling, Substrate noise coupling, Signal noise coupling, Examples of optimized structures, Few applications of mixed signal ASICs:

Applications areas: A heart rate meter, Hearing aid ASIC, Sound and rhythm generator, TV picture in picture processor, A multi-standard modem, A speech scrambler de-scrambler.

References:

1. Analogue-digital ASICs: circuit techniques, design tools and applications, Edited by R.S. Soin, F. Maloberti and J. Franca, IEE Publications
2. Signal Integrity Effects in Custom IC and ASIC Designs, Raminderpal Singh (Editor), Wiley Publications

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Semester I

E 15(E) RISC Microcontrollers

Teaching SchemeExamination Scheme
Lectures: 3 Hrs./Week
Credit: 3 .

Unit- 1 PIC: Modern Architectures:

- Introduction: PIC microcontroller features, MPLAB IDE, PICmicro Architecture, Program memory, Instruction set, Instruction Format, Byte-Oriented Instructions, Bit-Oriented Instructions, Literal Instructions, Control Instructions (CALL and GOTO), Destination Designator (d), Addressing Modes

Unit- 2

- PIC micro Hardware: reset, clock, control registers, register banks, program memory paging, Ports, interrupts, Timer and Counter, watchdog timer, power up timer, sleep mode, state machine programming,

- MPLAB overview: Using MPLAB, Toolbars, Select Development Mode And Device Type, Project, Text Editor, Assembler, MPLAB Operations.

ARM :

Unit – 3

Introduction to Embedded System Design, Embedded System Architecture, Embedded System model, an overview of Programming Languages and xamples of their standards, Embedded Processor: ISA Architecture Models, CISC & RISC model, Instruction – Level Parallelism ISA model, Von Neumann & Harvard Architectures.

Unit – 4

ARM Embedded System, ARM Processor Fundamentals: Registers, Pipeline, Exceptions,Interrupts and vector tables, ARM Processor family, ARM Instruction Set, Thumb Instruction Set. Overview of C compiler and Optimization: Register allocation, Functions Calls, Pointer aliasing, Structure arrangement, Portability issues, writing and optimizing ARM assembly code

Unit –5

Interrupts and interrupt handling Scheme, firmware and Boot loader, Real-Time operating Systems: Context Switching, task tables and kernels, Time Slice,Scheduleralgorithms:RMS, Deadline monotonic Scheduling; Priority Inversion, Tasks, Threads and process,Exceptions, Exception handling

Unit –6

Introduction to DSP on ARM –FIR Filter – IIR Filter – Discrete fourier transform –
Exception Handling – Interrupts – Interrupt handling schemes- Firmware and bootloader

Books: (PIC)

1. PIC Microcontrollers : An Introduction to Microelectronics, Martin P. Bates, Elsevier. www.newnespress.com
2. Embedded Design with the PIC18F452, John B. Peatman,
3. Programming & Customizing PICmicro Microcontrollers, MykePredko, TMH.
4. PIC in Practice, David W Smith, Newnes.
5. PIC Microcontroller: An Introduction to Software & Hardware Interfacing, Han-Way Huang, Thomson.
6. PIC: Your Personal Introductory Course, John Morton, Newnes.

ARM

Text books:

1. Embedded Systems Architecture by Tammy Overgaard; Elsevier Publisher; 2005
2. ARM System Developer's Guide by A.N. Sloss, D. Symes and C. Wright; Elsevier Publisher; 2006

Reference books:

1. Embedded System Design by Steve Heath, Elsveir Publisher; 2006
2. Embedded Systems by Raj Kamal, TMH; 2006
3. Embedded Microcomputer Systems, Thomson Publisher; 2005
4. Embedded system Design, Kluwer Academic Publisher; 2005
5. An Introduction to the design of small-scale embedded Systems by T. Wilmshurst, Palgrav publisher; 2001

SHIVAJI UNIVERSITY
M.TECH (Electronics Technology) PROGRAMMES

Semester I

E15 (E)AUTOMOTIVE EMBEDDED SYSTEMS

Teaching SchemeExamination Scheme
Lectures: 3 Hrs./Week
Credit: 3

Unit 1
Current trends in Automobiles, open loop and closed loop systems - components for electronic engine management system. Electro magnetic interference suppression. Electromagnetic compatibility, Electronic dashboard instruments, onboard diagnostic system , **6hrs.**

Unit 2
security and warmingsystem. Electronic management of chassis systems.Vehicle motion control.Sensors and actuators,and their interfacing. Basic sensor arrangement, types of sensors such as- oxygen sensors, crankangle position sensors- Fuel metering/ vehicle speed sensors and destination sensors, Attitude sensor,Flow sensor, exhaust temperature, air mass flow sensors. Throttle position sensor **7hrs.**

Unit 3
solenoids, steppermotors, relays. Electronic ignition systems.Types of solid state ignition systems and their principleof operation. **6hrs.**

Unit 4
Digital engine control system. Open loop and closed loop control system, Enginecranking and warm up control. Acceleration enrichment. Deceleration learning and ideal speedcontrol, Distributor less ignition – Integrated engine control system, Exhaust emission controlengineering. **7hrs.**

Unit 5
Automotive Embedded systems. **6hrs.**
PIC, Freescale microcontroller based system. Recentadvances like GLS, GPSS, GMS. Multiprocessor communication using CAN bus.

Unit 6
Case study- cruisecontrol of car. Artificial Intelligence and engine management **7hrs.**

References:
1. William B. Riddens, "Understanding Automotive Electronics", 5th Edition, Butterworth Hennimann Woburn, 1998.
2. Young A.P. & Griffiths, " Automotive Electrical Equipment" , ELBS & New Press-1999.
3. Tom Weather Jr. &Cland c. Ilunter, " Automotive computers and control system" Prentice Hall Inc., New Jersey.
4. Crouse W.H., " Automobile Electrical Equipment" , McGraw Hill Co. Inc., New York ,1995.
5. Bechhold, " Understanding Automotive Electronic", SAE,1998.
6. Robert Bosch," Automotive Hand Book", SAE (5TH Edition),2000.

SHIVAJI UNIVERSITY
M.TECH (Electronics Technology) PROGRAMMES

Semester II

C 21 DSP Processors

Teaching SchemeExamination Scheme
Lectures: 4 Hrs./Week
Credit: 4
Practical:2Hrs/week
Credit: 1

Unit 1: **6hrs.**
Architecture and instruction set of DSP processor
Introduction to TMS320C6x processor, architecture, pipelining, linear and circular addressing modes, TMS320C6x instruction set, assembler directives, timers, interrupts, serial I/O, DMA, fixed and floating point data format,

Unit 2: **7hrs.**
Digital signal processing and DSP systems: Advantages of DSP, characteristics of DSP systems, DSP applications. DSP processors, architecture and instruction set.

Unit 3: **6hrs.**
Numeric representations and arithmetic: floating point numbers, IEEE 754 standard for floating point numbers,

Unit 4:
Memory Architectures: memory structures, wait states, extended memory interfaces, addressing mechanisms.

Unit 5: **7hrs.**
Execution control: Hardware looping, interrupts, stack, relative branch support
Pipelining: pipelining and performance, pipelining depth, interlocking, branching effects, interrupt effects,

Unit 6: **6hrs.**
Peripherals: serial / parallel ports, timers, communication ports, on-chip A^D and D/A converters,-external interrupts, on-chip debugging facilities, power consumption, clocking.

Books:

1. DSP Processor Fundamentals: architectures and Features, by Phil Lapsley, Wiley 2. DSP Applications using C and the TMS320C6x DSP

.

Semester II

C22 REAL TIME OPERATING SYSTEMS

Teaching SchemeExamination Scheme
Lectures: 4 Hrs./Week
Credit: 4
Practical:2Hrs/week
Credit: 1

Unit 1: **6hrs.**
Software Architectures, Software Developments Tools, Programming Concepts, Embedded Programming in C and C++

Unit 2: **7hrs.**
Queues, Stacks, Optimization of Memory needs, Program Modeling Concepts, Software Development Process Life Cycle and its Model, Software Analysis, Design and Maintenance, Operating System Concepts

Unit 3: **6hrs.**
Processes, Deadlocks, Memory Management, Input /Output, Files, Security, the Shell, Recycling of Concepts. Operating system structure Monolithic Systems: Layered Systems, Virtual Machines, Exo-kernels, Client-Server Model

Unit 4: **7hrs.**
Real Time Operating Systems (μC/OS):Real-Time Software Concepts, Kernel Structure, Task Management, Time Management, Inter task Communication & Synchronization, Memory Management, and Porting μCos-II. REAL TIME KERNEL Principles – Design issues – Polled Loop Systems – RTOS Porting to a Target – Comparison and study of various RTOS like QNX – VX works – PSOS – C Executive – Case studies.

6hrs.

Unit 5:
Linux/RT Linux: Features of Linux, Linux commands, File Manipulations, Directory, Pipes and Filters, File Protections, Shell Programming, System Programming, RT Linux Modules, POSIX Threads, Mutex Management, Semaphore Management. **7hrs.**

Unit 6:
RTOS APPLICATION DOMAINS vizRTOS for Image Processing – Embedded RTOS for voice over IP – RTOS for fault Tolerant Applications – RTOS for Control Systems.

References:

1. μC/OS-II, The real time Kernel, Jean J. Labrossy, Lawrence: R & D Publications.
2. Embedded Real Time Systems: Concepts, Design & Programming, Dr.K.V.K.K. Prasad, Dreamtech Publication.
3. An Embedded Software Primer, David E. Simon, Pearson Education Publication.
4. Modern Operating Systems, Second Edition, Andrew S. Tanenbaum, Prentice Hall Publication.

SHIVAJI UNIVERSITY
M.TECH (Electronics Technology) PROGRAMMES
Semester II

C 23 High Speed Digital Design

Teaching SchemeExamination Scheme
Lectures: 4 Hrs. /Week
Credit: 4
Practical: 2Hrs./Week
Credit: 1

Unit 1: High Speed ADCs **6hrs.**

Fundamental of high speed sampling, Base band antialiasing filters, Study of Harmonic sampling and band pass sampling, Direct IF to digital conversion, Distortion and noise in an ideal N bit ADC, AD9220 12 bit ADC, Spurious free Dynamic Range, Measurement of Noise Power Ratio, Flash converters, Case study of AD9066, Study of latency of ADCs,

Unit 2: High Speed ADC Applications **7hrs.**

Driving ADC inputs for low distortion and wide dynamic range, Applications of high speed ADCs in CCD imaging, High speed ADC applications in Digital transceivers

Unit 3: High Speed DACs and DDS Systems **6hrs.**

Introduction to DDS, Aliasing in DDS Systems, 125 MSPS DDS System case study AD9850, DDS systems as ADC Clock Drivers.

Unit 4: **7hrs.**

Amplitude modulation in a DDS System, The AD9831 Complete DDS System, High Speed low distortion DAC architecture, High Speed interpolating DACs, QPSK signal generation using DDS

Unit 5: Design issues of high speed Electronics **6hrs.**

Simulation tools, Prototyping Circuits, Grounding in high speed systems.

Unit 6: **7hrs.**

Power supply noise reduction and filtering, Power supply conditioning, EMI/RFI considerations, Shielding concepts

Reference Books:

1. High-Speed Digital Design: A Handbook of Black Magic by Howard Johnson
2. High Speed Signal Propagation: Advanced Black Magic by Howard W. Johnson
3. Signal Integrity Issues and Printed Circuit Board Design by Douglas Brooks
4. High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices by Stephen H. Hall
5. Signal Integrity - Simplified by Eric Bogatin
6. Handbook of Digital Techniques for High-Speed Design : Design Examples, Signaling and Memory Technologies, Fiber Optics, Modeling, and Simulation to Ensure ... (Prentice Hall Modern Semiconductor Design) by Tom Granberg
7. Noise Reduction Techniques in Electronic Systems, 2nd Edition by Henry Ott
8. High Speed Design Techniques, Manual by analog Devices, October 1996

Semester II

C 24 DSP Processor Lab

Pratical : 2 hrs./week **Credit :** 1

Students are instructed to frame and perform laboratory assignments, based on each of theory course. The assignment should encompass the hardware techniques and software tools introduced in the concerned subjects and should prove to be useful for the PG programs in the relevant discipline. Assignment should be a full-fledged system design type problem with multi-dimensional solutions suggested. Assignment should be implemented using known hardware techniques/software tools and should be reliably executable.

Student shall submit a laboratory work document based on these assignments performed at the end of semester. The Laboratory instructor shall guide the students in framing the assignments and defining the problem pertaining to the said subjects.

SHIVAJI UNIVERSITY

M.TECH (Electronics Technology) PROGRAMMES

Semester II

C 25 Real Time Operating System Lab

Pratical : 2 hrs./week **Credit :** 1

Students are instructed to frame and perform laboratory assignments, based on each of theory course. The assignment should encompass the hardware techniques and software tools introduced in the concerned subjects and should prove to be useful for the PG programs in the relevant discipline. Assignment should be a full-fledged system design type problem with multi-dimensional solutions suggested. Assignment should be implemented using known hardware techniques/software tools and should be reliably executable.

Student shall submit a laboratory work document based on these assignments performed at the end of semester. The Laboratory instructor shall guide the students in framing the assignments and defining the problem pertaining to the said subjects.

SHIVAJI UNIVERSITY

M.TECH (Electronics Technology) PROGRAMMES

Semester II

C 26 High Speed Digital Design Lab

Pratical : 2 hrs./week **Credit :** 1

Students are instructed to frame and perform laboratory assignments, based on each of theory course. The assignment should encompass the hardware techniques and software tools introduced in the concerned subjects and should prove to be useful for the PG programs in the relevant discipline. Assignment should be a full-fledged system design type problem with multi-dimensional solutions suggested. Assignment should be implemented using known hardware techniques/software tools and should be reliably executable.

Student shall submit a term-work document based on these assignments performed at the end of semester. The Laboratory instructor shall guide the students in framing the assignments and defining the problem pertaining to the said subjects.

SHIVAJI UNIVERSITY
M.TECH (Electronics Technology) PROGRAMMES

Semester II

Elective-I

E 24 (V)Systems on Chip

Teaching SchemeExamination Scheme
Lectures: 3 Hrs./Week
Credit: 3

Unit 1: **6hrs.**
IC Technology, Economics, CMOS Technology overview, Power consumption, Hierarchical design, Design Abstraction, EDA tools.

Unit 2: **7hrs.**
MOSFET model, parasitics, latch up, advanced transistor structures; Wire parasitics; Design rules, Scalable design rules, process parameters; stick diagrams, Layout design tools; Layout synthesis, layout analysis.

Unit 3: **6hrs.**
CMOS gate delays, transmission time, speed power product, low power gates; Delay by RC trees, cross talk, RLC delay, cell based layout, Logic & interconnect design, delay modeling, wire sizing; Power optimization, Switch logic networks.

Unit 4: **7hrs.**
Pipelining, Data paths, Adders, ALUs, Multipliers, High density memories; Metastability, Multiphase clocking; Power optimization, Design validation, Sequential testing; Architecture for low power.

Unit 5: **6hrs.**
Floor planning methods, global routing, switch box routing, clock distribution; off chip connections, packages, I/O architectures, pad design.

Unit 6: **7hrs.**
Complete chip design including architecture, logic and layout for Kitchen timer chip OR Microwave oven chip

Reference books:

1. Wayne Wolf, "Modern VLSI Design", Pearson Education.

2. *KamaranEshraghian, "Principles of CMOS VLSI Design", Pearson Education*

3. *Rabey, Chandrakasan, "Digital IC Design", Pearson Publication*

Semester II

E 24 (V) Wavelet Transform and its applications

Teaching SchemeExamination Scheme
Lectures: 3 Hrs./Week
Credit: 3

Unit 1.Continuous wavelet Transform **6hrs.**

Introduction, Continuos-Time Wavelets, Definition of the CWT, The CWT as a Correlation. Constant Q - Factor Filteing Interpretation and Time-Frequency resolution, The CWT as an Operator, Inverse CWT.

Unit 2. Introduction to the Discrete Vavelet Transform and Orthogonal-Vavelet Decomposition **7hrs.**

Introduction, Approximation of Vectors in Nested Linear Vector Subspaces,
(i) Example of Approximating Vectors in Nested Subspaces of a Finite-Dimensional Linear Vectors Space,
(ii) Example of Approximating Vectors in Nested Subspaces of an infinite- Dimensional Linear Vectors space,
Example of an MRA, **(i)** Bases for the Approximation subspaces and Haar Scaling function,
(ii) Bases for the Detail Subspaces and Haar Wavelet,
(iii) Digital Filter Implementation of the Haar Wavelet Decomposition.

Unit3. NIRA, Orthonormal -Vavelets, and their Relationship to Filter Banks **6hrs.**

Introduction, Formal Definition of an MRA, Construction of a General Orthonormal MRA,
(i) Scaling Function and Subspaces,
(ii) Implication of the Dilation Equation and Ortliogonality,
A wavelet Basis for the MRA
(i) Two scale Relation for (t),
(ii) Basis for the detail subspaces
(iii) Direct sum decomposition,
Digital Filtering interpretation.
(i) Decomposition Filters,
(ii) Reconstructing the Signal.
Examples of Orthogonal Basis-Generating Wavelets,
(i) Daubechies D4 Scaling Function and Wavelet,
(ii) Band limited Wavelets, Interpreting Orthonormal MRAs for 40 Discrete-Time Signals,
(i) Continuous-Time MRA interpretation for DTWT,
(ii) Discrete-Time MRA,
(iii) Basis Functions for the DTWT, Miscellaneous issues related to PRQMF Filter Banks, Generating Scaling Functions and Wavelets from Filter Coefficients

Unit4. Alternative Wavelet Representations **7hrs.**

Introduction, Biorthogonal Wavelet Bases, Filtering Relationship for Biorthogonal Filters, Examples of Biorthogonal Scaling Functions and Wavelets, Two-Dimensional Wavelets, Nonseparable Multidimensional Wavelets, Wavelet packets.

Unit5. Wavelet Transform and Data Compression **6hrs.**

Introduction, Transform coding, DTWT for Image Compression,
(i) Image Compression using DTWT and Run-Length Encoding,
(ii) Embedded Tree Image Coding,
(iii) Comparison with JPEG, Audio Compression.
(I) Audio Masking,
(ii) Standards Specifying Subband Implementation: ISO/MPEG Coding for Audio,
(iii) Wavelet-Based Audio Coding, Video Coding Using Multiresolution Techniques: A Brief Introduction.

Unit6. Other Applications of Wavelet Transforms **7hrs.**

Introduction, Wavelet Denoising, Speckle Removal, Edge Detection and Object Isolation, Image Fusion, Object Detection by Wavelet Transforms of Projrctions, Communication Applications,
(i) Scaling Functions as Signaling Pulses,
(ii) Discrete Wavelet Multitone Modulation

1.

Text Book:

1. Wavelet Transforms - Introduction to Theory & Applications, RaguhuveerM.Rao&Ajit S. Bopadikar - Addison Wesley-1998

Reference Book:

1. Wavelets and Filter Banks, Gilbert Stang& Truong Nguyen-Wellesly -1996

References :

1.P. P. Vaidyanathan: Multirate Systems & Filter Banks, PTR, PH, 19932.Gilbert Strang : Linear Algebra and its Applications.3.Reghuveer M Rao, Ajit S Bopardikar: Wavelet Transforms

2. Introduction to Theory and Applications, Pearson Education Asia, 1998.4.Strang G S, T Q Nguyen:Wavelets and Filter Banks,

3. WellesleyCambridge Press 1996.5.Burrus C S, R A Gopinath and H. Gao: Introduction to Wavelets and Wavelet Transforms: APrimer , Prentice Hall, 1998.

SHIVAJI UNIVERSITY
M.TECH (Electronics Technology) PROGRAMMES

Semester II

E 24 (E) Microelectromechanical Systems

Teaching SchemeExamination Scheme
Lectures: 3 Hrs./Week
Credit: 3

Unit 1: **6hrs.**
History of MicroElectroMechanical Systems (MEMS), market for MEMS, basics of microtechnology, lithography and etching techniques,

Unit 2: **7hrs.**
principles of bulk and surface micromachining: subtractive processes, additive processes (evaporation, sputtering, epitaxial growth). Fundamental devices and processes, Multi User MEMS Process (MUMPs), SUMMiT: design rules; applications; micro hinges and deployment actuators,

Unit 3: **6hrs.**
CMOS MEMS, cleanroom lab techniques, MicroOptoElectroMechanical Systems (MOEMS), bioMEMS and biomaterials, piezoresistivity; scanning probe microscopy, scaling laws, applications.

Unit4: **7hrs.**
Lumped element modeling and design, Electrostatic Actuators , Electromagnetic Actuators, Linear and nonlinear system dynamics, resonant systems, Elasticity (stress, strain, material properties), Mechanical structure basics (bending of bes, torsion,natural frequency), Optical system design basics (Gaussian beam optics, matrix optics, resolution)

Unit 5: **6hrs.**
Application case studies: MEMS Scanners and Retinal Scanning Displays (RSD), Grating Light Valve (GLV), Digital Micromirror Devices (DMD),

Unit 6: **7hrs.**
Optical switching, Capacitive Micromachined Ultrasonic Transducers (CMUT)

Reference Books:

1. Gregory T A 1998, Kovacs Micromachined Transducers Sourcebook, WCB McGraw-Hill.
2. NadimMaluf, An introduction to Microelectromechanical system design, Artech House, 2000
3. Victor M. Bright, Editor, Selected papers on Optical MEMS, SPIE Milestone Series, Volume MS 153, SPIE Press, 1999
4. Mohamed Gad-el-Hak, Editor, The MEMS Handbook, CRC Press, Baco Raton, 2001
5. Marc Madou, Fundamentals of Microfabrication, CRC Press, New York, 1997.
6. Gregory T. A. Kovacs, Micromachined Transducers Sourcebook, WCB / McGraw-Hill
7. W. Trimmer, Editor, Micromechanics and MEMS: Classic and Seminal Papers to 1990, IEEE Press, 1996

SHIVAJI UNIVERSITY
M.TECH (Electronics Technology) PROGRAMMES

Semester II

E 24 (E) Robotics and Machine Vision

Teaching SchemeExamination Scheme
Lectures: 3 Hrs./Week
Credit: 3

UNIT 1 **6hrs.**
Robotics – Introduction–Basic Structure– Classification of robot and Robotic systems –laws of robotics – robot motions – work space, precision of movement.
Drives and control systems: Hydraulic systems, power supply – servo valve – sump – hydraulic motor – DC servo motors – stepper motors – operation.
Mechanical Components of Robots: Power transmission systems: Gear transmission. Belt drives, cables, Roller Chains, Link – Road Systems, Rotary to linear motion conversion, Ract and pinion drives, ball bearing screws, speed reducers, Harmonic drives.

UNIT 2 **7hrs.**
Kinematics of Robot: Introduction, Matrix Representation, Homogeneous transformation, forward and inverse Kinematics, Inverse Kinematics Programming, Degeneracy, dexterity, velocity and static forces, velocity transformation force control systems, Basics of Trajectory planning.

UNIT 3 **6hrs.**
Robot End Effectors: Types of end effectors – Mechanical grippers – Types of Gripper mechanisms – Grippers force analysis – Other types of Grippers – Vacuum cups – Magnetic Grippers – Adhesive Grippers – Robot end effector interface.
Sensors: Position sensors – Potentiometers, encoders – LVDT, Velocity sensors, Acceleration Sensors, Force, Pressure and Torque sensors, Touch and Tactile sensors, Proximity, Range and sniff sensors, RCC, VOICE recognition and synthesizers.

UNIT 4
Machine Vision: Introduction – Image processing Vs image analysis, image Acquisition, digital Images – Sampling and Quantization – Image definition, levels of Computation. **7hrs.**

UNIT5 Image processing Techniques: Data reduction – Windowing, digital conversion. **6hrs.**
Segmentation – Thresholding, Connectivity, Noise Reduction, Edge detection, Segmentation, Region growing and Region Splitting, Binary Morphology and grey morphology operations.

UNIT 6 **7hrs.**
Feature Extraction: Geometry of curves – Curve approximation, Texture and texture analysis, Image resolution – Depth and volume, Color processing, Object recognition by features, Depth measurement, specialized lighting techniques. Segmentation using motion – Tracking. Image Data Compression, Real time Image processing, Application of Vision systems.

TEXT BOOK

1.Saeed B. Niku, Introduction to Robotics: Analysis, Systems, Applications, 2nd edition, Pearson Education India, PHI 2003 (ISBN 81-7808-677-8)

REFERENCES

1. M.P. Groover, Industrial Robotics – Technology, Programming and Applications, McGraw-Hill, USA, 1986.
2. Ramesh Jam, RangachariKasturi, Brain G. Schunck, Machine Vision, Tata McGraw-Hill, 1991.
3. Yoremkoren, Robotics for Engineers, McGraw-Hill, USA, 1987.
4. P.A. Janaki Raman, Robotics and Image Processing, Tata McGraw-Hill, 1991.

SHIVAJI UNIVERSITY
M.TECH (Electronics Technology) PROGRAMMES

Semester II

Elective –II

E25(V) RF Integrated Circuit Design

Teaching SchemeExamination Scheme
Lectures: 3 Hrs./Week
Credit: 3 .

Unit 1: **6hrs.**
Introduction to MOSFET Devices, MOSFET modeling, Spice model, Device parasitics, RF modeling, Parasitics sensitive to RF.

Unit 2: **7hrs.**
Issue in RF IC a brief review, Impedance matching, use anddesign of passive circuits, LNA Design.

Unit 3: **6hrs.**
Matching Techniques using algebra techniques, Basic Bondcircuits, UHF Mixer design.

Unit 4: **7hrs.**
Cross talk, Cross connect architecture, Cross Connect characteristics,classification, Cross connect mechanism, Cross connect mitigation, Cross connect reduction,
multiple Cross connect sources.

Unit 5: **6hrs.**
EMI, EMC, Importance in ASIC Design, Introduction, EDA Tool inASIC Design,

Unit 6: **7hrs.**
Design Flow, testing, Environment, sources of EMI/RFI, Solutions.

References
1. Thomas Lee, " RF IC Design" Oxford Press..
2. T. Yettrdal, Yunhg Cheng, "Devices modeling for analog and RF COMS circuitsdesigne", John Wiley publication 2003.
1. Calvin Plett, "Radio frequency Integrated Circuits Design", Artech house.

SHIVAJI UNIVERSITY
M.TECH (Electronics Technology) PROGRAMMES

Semester II

E 25 (V) VLSI in Signal Processing

Teaching SchemeExamination Scheme
Lectures: 3 Hrs./Week
Credit: 3

Unit 1:
Typical DSP algorithms and representation : DCT, DWT and filter banks, Vector Quantization, Block diagram, signal flow graph, data flow graph and dependence graph. **6hrs.**

Unit 2:
DSP application demands and CMOS technologies, Loop bound and iteration bound and their computation, Pipelining and Parallel Processing: Pipelining of FIR Digital filters, parallel FIR digital filters, combined pipelining and parallel processing. **7hrs.**

Unit 3:
Retiming, Properties of retiming, Retiming techniques for clock minimization and register minimization. Unfolding, properties and applications of unfolding. **6hrs.**

Unit 4:
Folding, 2D Systolic arrays and matrix multiplication, Bit level arithmetic architectures: Parallel multipliers, Baugh Wooley carry save multiplier, Booth Wallace Tree multipliers, Bit serial multipliers, Bit serial FIR filter. Carry free radix-2 addition and subtraction, **7hrs.**

Unit 5:
Floating point arithmetic, Clocking for synchronous pipelining and wave pipelining systems, Clock distribution, Floor planning. **6hrs.**

Unit 6:
FPGA architectures: block memories, CLBs, IOBs, Routing resources, specific resources like MAC, DLL, clock managers etc. **7hrs.**

References books:

1. *"VLSI Digital Signal Processing Systems, Design and Implementation" by KeshabParhi, John-Wiley & sons.*
2. *"Principles of CMOS VLSI Design", by Neil H.E.Weste, Kamran Eshraghian, Pearson Education.*
3. *"Digital Systems Desoign Using VHDL", by Charles Roth, Jr. Thomas Learning.*
4. *"Design Warriors guide to FPGAs" by C.M Maxfield, Newness.*
5. *"Digital Signal Processing with Field Programmable Gate Arrays", U.Meyer-Baese, second edition Springer*

Semester II

E 25 (E)High Performance Networks

Teaching SchemeExamination Scheme
Lectures: 3 Hrs./Week
Credit: 3

Unit 1: **6hrs.**
Types of Networks, Network design issues, Data in support of network design.Network design tools, protocols and architecture.

Unit 2: **7hrs.**
VoIP system architecture,protocol hierarchy, Structure of a voice endpoint, Protocols for the transport ofvoice media over IP networks. Providing IP quality of service for voice, signaling protocols for VoIP, PSTN gateways, VoIP applications.

Unit 3: **6hrs.**
Introduction, challenges,SCSI protocols and architecture: RAID, Backup and mirroring, Fiber channelattached storage. Network attached storage including NFS, CIFS and DAFS,
Management of network storage architectures.New storage protocols,architectures and enabling technologies.

Unit 4: **7hrs.**
Introduction to CDMA and spreadspectrum system, CDMA standards, system architectures of wirelesscommunication systems, physical, network and data link layer of CDMA, wireless LAN standards: IEEE 802.11b, ARPA.

Unit 5: **6hrs.**
Overview of Information Theory. LosslessCompression: Run-Length Encoding, Facsimile compression, String-matchingAlgorithms.Lossy Compression: DCT, Wavelet compression.

Unit 6: **7hrs.**
A model for internet security, security attacks, services, internet standards &RFCs, Cryptography, Conventional encryption, principles and algorithms, cipherblock,modes of operation, location of encryption devices , key distribution,Public key cryptography principles and algorithms, RSA algorithm.

Reference Books :

1. Kershenbaum A., "Telecommunications Network Design Algorithms", Tata McGraw Hill.
2. Ramaswami R., Shivrajan K, "Optical Networks", Morgan Kaufmann.
3. Douskalis B., "IP Telephony: The Integration of Robust VoIP Services", Pearson Ed. Asia.
4. Warland J., Varaiya P., "High-Performance Communication Networks", Morgan Kaufmann, 1996.
5. Stallings W., "High-Speed Networks: TCP/IP and ATM Design Principles", Prentice Hall,1998.

6. Garg V., Smolk K., VilkesJ.,"Applications of CDMA in wire less communication".
7. William Stalling : Network security, essentials- Pearson education Asia publication.

Semester II

E 25 (E) Mobile Computing

Teaching SchemeExamination Scheme
Lectures: 3 Hrs./Week
Credit: 3

Unit 1: **6hrs.**
1G to 4G mobile telephone technologies.

Unit 2: **7hrs.**
Reference architectures for wireless LAN, WLANGPRS.

Unit 3: **6hrs.**
GSM and VOIP architecture, 4-G LTE network architecture and protocols

Unit 4: **7hrs.**
Transmitdiversity and MIMO spatial multiplexing,

Unit 5:
Applications of Mobile computing Business valuebehind mobile application development Best practices for the entire project life cycle. **6hrs.**

Unit 6: **7hrs.**
Casestudies secure mobile application development Fundamentals of wireless Mark up language WML script applications.

Reference Books:

1. Introduction to Mobile Telephone Systems, 2nd Edition, 1G, 2G, 2.5G, and 3G Technologies and Services by Lawrence Harte
2. Wireless and Mobile Data Networks by Aftab Ahmad
3. Wireless and Mobile Network Architectures by Yi-Bing Lin and ImrichChlamtac
4. Mobile Applications: Architecture, Design, and Development by Valentino Lee, Heather Schneider, and Robbie Schell
5. Mobile IP Technology and Applications by Stefan Raab and Madhavi W. Chandra
6. Mobile Application Security [Paperback] HimanshuDwivedi (Author), Chris Clark , David Thiel
7. Beginning WAP: Wireless Markup Language & Wireless Markup Language Script by SooMee Foo, Ted Wugofski, Wei Meng Lee, and Foo SooMee
1. WML &WMLScript: A Beginner's Guide by Kris A. Jamsa

Semester I & II

S 16 & S 26 Seminars

Teaching SchemeExamination Scheme
Contact hrs : 2 Hrs./Week/student
Credit: 2

Students shall deliver Seminar on the State-of-the-Art topic in front of Examiners and Student-colleagues. Prior to presentation, he/she shall carry out the detailed literature survey from Standard References such as International Journals and Periodicals, recently published reference Books etc. and submit a report on the same along with computer based presentation copy to the concerned examiner/guide at the end of the seminar. The assessment shall be based on selection of topic, its relevance to the present context, report documentation and presentation skills.

Guide should spare(Guide) for 2hrs /week/student for seminar

SHIVAJI UNIVERSITY
M.TECH (Electronics Technology) PROGRAMMES

Semester-III

T 31 Industrial Training:

Teaching SchemeExamination Scheme
Contact hrs : 2 Hrs./Week/student
Credit: 4

8 Weeks at the end of First Year and as a part of evaluation at the end of third semester student should submit the report for the 8 week industrial training and give presentation to the concern guide, concern guide should spare 2hrs/week/student

SHIVAJI UNIVERSITY

M.TECH (Electronics Technology) PROGRAMMES

Semester-III & IV

S 32 and D 42 Dissertation Project Phase I & II

The student shall be allowed to submit the dissertation phase I report only after the completion of minimum 50% work of the total project with intermediate /partial results of the dissertation project to the concern guide and the dissertation phase II report only after the full-fledge demonstration of his /her work to the concerned guide. Assessment of the dissertation shall be based on design & implementation aspects, documentation & presentation skills, utility of the dissertation work & publications based on the same.

For the dissertation phase I and phase II concern guide should guide to each student minimum for **2** hrs per week till the final submission of the dissertation of the concern student.

SHIVAJI UNIVERSITY

M.TECH (Electronics Technology) PROGRAMMES

Equivalence of M. Tech (Electronics Technology) Semester I and II

Semester I

Course Code	M. Tech (Electronics Technology) Semester I Pre-revised syllabus	Course Code	M. Tech (Electronics Technology) Semester I & II Revised syllabus
C11	CMOS VLSI Design	C11	CMOS VLSI Design
C12	Digital Systems Testing and Simulation with VHDL	E15(V)	Digital System and Testing
C13	High Speed Analog Design Techniques	E25(V)	High Speed Analog Design Techniques
E 14	Elective –I (PIC ARM and AVR)	C13	RISC Microntrollers
E 15	Elective –II (Embedded C and RTOs	C22	Real Time Operating System

Semester II

Course Code	M. Tech (Electronics Technology) Semester II Pre-revised syllabus	Course Code	M. Tech (Electronics Technology) Semester I & II Revised syllabus
C 21	DSP Processor Fundamentals	C 21	DSP Processor
C 22	High Speed Digital Design Techniques	E14(V)	High Speed Digital Design Techniques
C 23	Advanced Computer Networks	E15(E)	Communication Networks
E 24	Elective –III (Design using FPGA and VHDL)	C12	Reconfigurable Platforms & HDL
E 25	Elective –IV(DSP Algorithms and Applications	C 23	VLSI in Signal Processing

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M.TECH (Electronics Technology) PROGRAMMES

M. Tech (Electronics Technology)- Semester III

Sr. No	M. Tech (Electronics Technology) Semester III Pre-revised syllabus	M. Tech (Electronics Technology) Semester III Revised syllabus
1	Industrial Training	Industrial Training
2	Dissertation Phase – I	Dissertation Phase-I

M. Tech (Electronics Technology)- Semester IV

Sr. No	M. Tech (Electronics Technology) Semester IV Pre-revised syllabus	M. Tech (Electronics Technology) Semester IV Revised syllabus
1	Dissertation Phase – II	Dissertation Phase-II