SHIVAJI UNIVERSITY
M.Tech. in Electronics
Introduced from June, 2006

ADMISSION TO M. TECH. PROGRAMMES

A. Eligibility Criteria

1) The qualifying criteria for the M.Tech. course is as below.

1. Computer Science and Engineering

B.E. / B.Tech. (CSE/CT/CE/CS/IT/ Electronics/ Electrical)
M.Sc. (CS/ IT)
AMIE / IETE

2. Environmental Science and Technology

B. E. / B. Tech. (Cvil/ Chemical/ Environmental)
AMIE / IETE
M. Sc. (Environmental Science)

3. Energy Technology

B. E. / B. Tech. (Mechanical/ Automobile/ Production/ Chemical/ Electrical)
AMIE / IETE
M.Sc. (Electronics)

4. Electronics

B.E. / B. Tech. (ETC/ Electronics / Industrial Electronics)
AMIE / IETE
M. Sc. (Electronics)

B. Selection Basis :

Valid GATE Score.

Vacant seats, if any shall be filled up from the merit list prepared by conducting written test and interview by the University.

SHIVAJI UNIVERSITY

M.TECH PROGRAMMES

A. Computer Science and Engineering
B. Environmental Science and Technology
C. Energy Technology
D. Electronics.

1. Programme Duration : Two Years : Four Semesters

2. Intake : 18 per Programme

3. Programme structure and syllabus

First Year -

a. Theory Subjects :
   6 Compulsory Subjects
   4 Elective Subjects

b. Practicals for compulsory Subjects
c. Seminars - 2
d. Industrial Training – 8 weeks at the end of the First Year. (Summer)

Second Year –
a. Dissertation

4. Scheme of Marking

a.	Theory Subjects	-	1000
b.	Practicals	-	300
c.	Seminars	-	100
d.	Industrial Training	-	100
e.	Dissertation	-	500
	Total		**2000**

5. Eligibility : As per AICTE norms.

Structure and Syllabus of M.Tech. Electronics

Scheme of study and syllabus of Shivaji University M.Tech programme in Electronics 2006-2007.M.Tech (Electronics) with two specializations one in Embedded Systems and other in VLSI Design

Eligibility: - B.E. in E and TC, B.E. in Electronics, B.E in Industrial Electronics, B.Tech in
Electronics and M.Sc.in Electronics.
Intake: - 18 as per AICTE rules

Scheme of study: -

SHIVAJI UNIVERSITY, KOLHAPUR

M.Tech. (Electronics)
Course Structure and Scheme of Evaluation
Semester-I

Course code	Name of the subject	Teaching Scheme		Examination Scheme		Total Marks
		Lectures	Practicals	Theory	Term Work	
C 11	CMOS VLSI Design	4	2	100	50	150
C 12	Digital Systems Testing and Simulation with VHDL	4	2	100	50	150
C 13	High Speed Analog Design Techniques	4	2	100	50	150
E14	Elective -I	4	-	100	-	100
E15	Elective –II	4	-	100	-	100
S16	Seminar-I	----------	2	---------	50	50
Total		20	08	500	200	700

Total Hrs. 28 , Total Marks 700

Elective-I
E 14 (V) Mixed Signal ASIC Design
E 14 (E) PIC ARM and AVR

Elective-II
E 15 (V) Analog and Low Power Digital VLSI Design
E 15 (E) Embedded C and RTOs

Specialization : V VLSI Design
E Embedded Systems

Semester-II

Course code	Name of the subject	Teaching Scheme		Examination Scheme		Total Marks
		Lectures	Practicals	Theory	Term Work	
C 21	DSP Processor Fundamentals	4	2	100	50	150
C 22	High Speed Digital Design Techniques	4	2	100	50	150
C 23	Advanced Computer Networks	4	2	100	50	150
E 24	Elective –III	4	-	100	-	100
E 25	Elective – IV	4	-	100	-	100
S 26	Seminar-II	----------	2	---------	50	50
Total		20	08	500	200	700

Total Hrs. 28 , Total Marks 700

Elective-I
E 24 (V) MicroElectromechanical Systems
E 24 (E) Design using FPGA and VHDL

Elective-II
E 25 (V) Mixed Signal ASIC Design
E 25 (E) DSP Algorithms and Applications

Semester-III

Course code	Name of the subject	Evaluation		Total Marks
		Term Work	Orals	
T31	* Industrial Training	100	--	100
S32	Dissertation Phase-I	100	100	200
Total		200	100	300

* 8 Weeks at the end of First Year (summer)

Semester-IV

Course code	Name of the subject	Evaluation		Total Marks
		Term Work	Orals	
D42	Dissertation Phase-II	100	200	300

Total Marks For Four Semesters: -

Semester	I	II	III	IV	**Total**
Marks	700	700	300	300	**2000**

M.Tech. in Electronics

C 11 CMOS VLSI Design

Unit 1: Introduction
VLSI Design: History, Trends, Principles, Metrics

Unit 2: Basics of CMOS
CMOS transistors (n-channel and p-channel), The CMOS Switch model, CMOS Inverter mode, Logic devices and interconnect, CMOS circuit analysis: transistors, inverters, interconnect modeling, parasitics, CMOS Process and Layout, CMOS Devices: SPICE and deep sub-micron issues

Unit 3: CMOS: Design Issues
CMOS Inverter: speed, power and scaling, Static CMOS Gates, Dynamic CMOS Gates, Power Estimation and Optimization

Unit 4: Modeling
Analytical modeling: Ellmore Delay, Transmission models, RC, RLC lumped parameter models, Layout for custom logic: Sea of Gates (SoG) model, Design rules, Circuit fabrication methods for CMOS, Levels of abstraction.

Unit 5: Circuits to Systems
VLSI circuits to systems, Circuit modeling and layout (demo using standard tools), CMOS design and layout tools, Nano-electronics circuits versus CMOS microelectronics circuits, Nano-computing techniques and device platforms

Unit 6: Digital IC Design
Digital CMOS IC design: Sequential Logic Circuits, Implementation Strategies for Digital ICs, Interconnects, Timing and Clocking, Datapath Design, Memory Design, Capactitive parasitics, Resistive parasitics, Inductive parasitics

Unit 7: Timing issues for Digital CMOS circuits
Timing Issues, Clock skew, clocking styles, Self-timed circuit design, Case study of Kitchen timer chip

Reference Books:

1. N.H.E. Weste and K. Eshraghian, "Principles of CMOS VLSI Design", New Uork: Addison-Wesley, 1993.
2. Christopher Saint and Judy Saint, "IC Layout Basics", McGraw Hill Publications
3. Weste and Harris, CMOS VLSI Design, a Circuits and Systems Perspective (3 rd edition)
4. by Jan M. Rabaey, A. Chandrakasan, B. Nikolic, Digital Integrated Circuits (2nd Edition) Prentice Hall, 2003.

C 12 Digital Systems Testing and Simulation with VHDL

Testing Defined: definitions and areas within testing. Logic and Fault Modeling.

Mechanics
Definitions: Abstractions level, Faults and errors, Modeling, Test Evaluation, Test Generation, Diagnostics.

System life, Sources of defects?
Representation and models of digital systems across abstraction levels.
Fault Models: logical versus physical; SSL model, opens and shorts, bridging faults; Basic assumptions.

Review of minimization tools and asynchronous machines, Test Pattern Generation basics. (activate and drive.), Algebraic approaches, Fault Equivalence and Dominance.

Test Generation: Algebraic Approaches and Structural Approaches, Logic Simulation.

Algebraic Approaches: Boolean difference, Literal position, Effect of fanout on circuits, Checkpoint faults.

Structural Approaches to test generation. Path sensitization methods.
Test Coverage
Logic simulations
Simulation engines: compiler, event driven. Representation of value, circuit, etc.

Logic and Fault Simulation: Delay models for circuit simulation, Fault Simulation Purpose of Serial and Parallel Fault Simulation, Deductive fault simulation. Concurrent Fault Simulation, Critical Path tracing, Statistical Fault Analysis

More Test Generation and D-algorithm
D-algorithm. representation, cube algebra, generalized algorithm, Extensions to D-algorithm PODEM, FAN, etc. Random test generation, Complexity issues

Functional Test Generation Methods, Heuristic Methods, Exhaustive and Pseudo Exhaustive techniques, Silberman's Difference Fault Model.

RAM and PLA testing, Microprocessor testing: Thatte and Abraham fault models and functional test generation.

Memory Testing: Memory test complexity, Memory fault models.

Design for Testability
Controllability and Observability measures. STEFAN, Ad Hoc techniques, More Design for Testability, Scan Design.

Scan Designs: IEEE Standards, Board-Level Testing: Boundary Scan, Data Compression and BIST, LFSR polynomial generation Data compression techniques
Aliasing Probability, BIST, Self Checking and PLD Testing
References:

1. "Digital Systems Testing and Testable Design" by Miron Abramovici, Melvin Breuer and Arthur Friedman, IEEE press, NY.
2. A Guide to VHDL'' by Stanley Mazor, Kluwer Academic Press
3. "HDL Chip Design" by Douglas Smith, Doone Publications, AL.
4. "Rapid Prototyping of Digital Systems", by J. O. Hamblen and M. Furman, Kluwer Academic Publishers.

C 13 High Speed Analog Design Techniques

Unit 1: High Speed Operational Amplifiers

Folded Cascode Voltage Feedback Op-Amps, Case study of AD847, Current Feedback Op-Amps (CFB), CFB model and Bode plot, study of AD8011, Comparison of specifications of Current feedback Op-amp family AD8001, AD8002, AD8009 and AD8073, Noise comparisons between VFB and CFB Op Amps, PSRR Characteristics.

Unit 2: High-Speed applications based on Op-amps

Optimizing feedback network for maximum bandwidth fitness, Driving Capacitive load, Cable drivers and receivers, High performance video line driver, Differential line drivers and receivers, High speed clamping amplifiers, High speed current to voltage converters and the effects of inverting input capacitance,

Unit 3: High speed amplifiers for communication applications

Low noise amplifiers for communication systems, Mixers, Power amplifiers, Liner drivers, Automatic gain control amplifiers

Unit 4: High speed system for video applications

High speed video multiplexing with Opamps using disable function, Video programmable gain amplifier, Video multiplexers and Cross Point switches, High power line drivers and ADSL, High speed photodiode Pre amps, Case studies of AD830, AD9002

Unit 5: High speed RF/IF Subsystems

Dynamic range compression, Linear VCAs, Log/Limiting Amplifiers, Receiver overview, Multipliers, modulators and mixers, Case study of AD600 Dual Channel X-amp, AD641 monolithic log amplifier.

Reference Books:

1. Intuitive Operational Amplifiers, Thomas M. Frederiksen, Mc Graw Hill, 1988.
2. B Razavi, "RF Microelectronics", Prentice Hall, 1998
3. T.H. Lee, "The Design of CMOS Radio-Frequency Integrated Circuits" Cambridge University Press, 1998.
4. High Speed Design Techniques, Manual by analog Devices, October 1996
5. Modular Low-Power, High Speed CMOS Analog-to-Digital Converter for Embedded Systems, Lin, Dr. Ing. Keh-La Kemma, Armin Hosticka, Prof. Bedrich J. Publisher, Kluwer Academic Publishers

E 14 (V) Mixed Signal ASIC Design

Unit 1: Technology and modeling aspects of an advanced BiCMOS ASIC process

LSI Logic analogue BiMOS technology, Background, Process technology, Well formation, Island definition and field region implants, Field oxidation - Island formation

Unit 2: High performance operational amplifiers and comparators

High performance amplifiers, The load compensated OTA (LC-OTA), The Miller compensated OTA (M-OTA), The core-amplifier (C-OTA), High performance comparators, The OTA as comparator, Latched comparators, A high speed accurate comparator.

Unit3: Switched current techniques for analogue sampled data signal processing

Introduction, First generation memory cells, Second generation memory cells, Limitations of the basic SI memory cell, Channel length modulation, Charge injection, Junction leakage Applications: Integrator based biquad, FIR filters, Sigma-Delta modulators

Unit 4: Data converters

Parameters for data converter characterisation, Data converters: Basic design considerations, High speed data conversion techniques, Current switched D/A converters, Flash and two-step flash converters, Limits to speed and resolution in data converters Oversampling converters, Intuitive Introduction to Oversampling Data Converters, Noise shaping converters, First order sigma delta modulators Second order sigma delta modulator, Multistage sigma-delta modulator, Non ideal effects in sigma delta modulators, Sampling jitter

Unit 5: Self-callibrating and algorithmic converters

Self-calibrated analogue-digital converters, Architecture with segmented binary-weighted capacitor Array, Self-calibration technique and circuits, Principle of calibration, Calibrating capacitors, Calibrating registers

Unit 6: A high flexibility BiCMOS standard cell library for mixed analogue-digital ASICs

A BiCMOS process dedicated to mixed A/D applications, Cell libraries, Analogue libraries, The digital cell library, CAD tools, The CAD capability, Telescopic Cells, Parametrizable cells, Adjustable cells, Automatic cell biasing and power down, ADS (Analog Design System) An environment for Mixed signal design, Analogue/digital multi-level mixed mode simulations

Unit 7: Case Studies:

Example 1: Infra red receiver with decoder and actuator
Example 2: Remote control

Unit 8: Advanced topics:

Element matching, Local process variations, Global process variations, Process gradients, Boundary effects, Noise coupling, Substrate noise coupling, Signal noise coupling, Examples of optimized structures

Unit 9: Few applications of mixed signal ASICs:

Applications areas: A heart rate meter, Hearing aid ASIC, Sound and rhythm generator, TV picture in picture processor, A multi-standard modem, A speech scrambler de-scrambler.

References:

1. Analogue-digital ASICs: circuit techniques, design tools and applications, Edited by R.S. Soin, F. Maloberti and J. Franca, IEE Publications
2. Signal Integrity Effects in Custom IC and ASIC Designs, Raminderpal Singh (Editor), Wiley Publications

E 14 PIC ARM and AVR

Modern Architectures:
PIC:

- Introduction: PIC microcontroller features, MPLAB IDE, PICmicro Architecture, Program memory, Instruction set, Instruction Format, Byte-Oriented Instructions, Bit-Oriented Instructions, Literal Instructions, Control Instructions (CALL and GOTO), Destination Designator (d), Addressing Modes (10)
- PICmicro Hardware: reset, clock, control registers, register banks, program memory paging, Ports, interrupts, Timer and Counter, watchdog timer, power up timer, sleep mode, state machine programming, (10)
- MPLAB overview: Using MPLAB, Toolbars, Select Development Mode And Device Type, Project, Text Editor, Assembler, MPLAB Operations. (5)

AVR:

- Introduction to AVR, Architecture and Hardware Resources of AVR Microcontrollers. (5)
- Architecture: The Arithmetic Logic Unit, Program and Data Memories, Downloadable Flash Program Memory, SRAM Data Memory, General-Purpose Register File, I/O Register, EEPROM Data Memory, Peripherals, Timer/Counter, Watchdog Timer, Serial Peripheral Interface SPI, Universal Asynchronous Receiver and Transmitter, Analog Comparator, I/O Ports, Reset and Interrupt System, Interrupt Vector Table, Reset Sources, Clock, Handling the Hardware Resources (5)
- AVR programming model and Instruction set: Memory Addressing Modes, Register Direct Addressing, I/O Direct Addressing, SRAM Direct Addressing, SRAM Indirect Addressing, Constant Addressing Using the LPM Instruction, Jumps and Calls, Instruction Set, Reset and Interrupt Handling, Watchdog Handling, Stack, Program Constructs, Conditional Branches, Program Loops, Refreshing Port Pins and Important Registers, Polling Inputs (15)
- Development Tools: ATMEL AVR Assembler and Simulator, ATMEL AVR Studio.

ARM Architecture:

Introduction to ARM processor and its important features, and Architecture

Programming model, Processor Operating State, Memory Formats, Instruction, Length, Data Types, Operating Modes, Exceptions and Interrupts Latencies and Reset.

Books (Interfacing)

1. The 8051 Microcontroller –K.J. Ayala, Penram International
2. Microcontroller – Jim Stewart, Psicataway, New Jersey, PHI.
3. Programming and Customizing the 8051 Microcontroller MYKE Predko, TMH, New Delhi.

Books: (PIC)

1. PIC Microcontrollers : An Introduction to Microelectronics, **Martin P. Bates, Elsevier.** www.newnespress.com
2. Embedded Design with the PIC18F452, **John B. Peatman**,
3. Programming & Customizing PICmicro Microcontrollers, **Myke Predko,** TMH.
4. PIC in Practice, **David W Smith**, Newnes.
5. PIC Microcontroller: An Introduction to Software & Hardware Interfacing, **Han-Way Huang**, Thomson.
6. PIC: Your Personal Introductory Course, **John Morton**, Newnes.

Books: (AVR)

1. Embedded C Programming and the Atmel AVR, **Richard H. Barnett, Sarah A. Cox, Larry D. O'Cull**, Thomson.
2. AVR: An Introductory Course, **John Morton**, Newnes.
3. AVR RISC Microcontroller Handbook, **Claus Kuhnel**, Newnes.
4. Programming and Customizing the AVR Microcontroller, **Dhananjay Gadre**, TMH.

A primer of microcontroller AVR, **Yoshio Kato**.

Books (ARM)

ARM Architecture Reference Manual, David Seal, Addison-Wesley.

E 15 (V) ANALOG and LOW POWER DIGITAL VLSI DESIGN

Unit 1: Low Power Design and Physics of Power Consumption, Power Estimation and Synthesis for low power, Design and test of low voltage CMOS circuits

Unit 2: Low power Static RAM architecture, Low power computing with energy recovery, Digital low power deign using hazard filters and balanced parities

Unit 3: Software design for low power

Unit 4: Case studies of Gilbert Cell Design with layout for low power

Unit 5: Case study of PLL design with layout for low power

Unit 6: Case study of $\sum$ - Δ A/D and D/A Converters for low power applications

Unit 7: Low power design for woreless circuits, Integrated radio frequency CMOS design

Reference Books:

1. Introduction to Low-Power VLSI Design (G Yeap & A Wild)
2. Low Power Design of Off-Chip Drivers and Transmission Lines: A Branch and Bound Approach (R Gupta et al.)
3. A New CMOS Driver Model for Transient Analysis and Power Dissipation Analysis (H Liao et al.)
4. On the Optimal Drivers of High-Speed Low Power ICs (D Zhou & X Y Liu)
5. Floorplan Design with Low Power Considerations (K-Y Chao & D F Wong)
6. Retiming Sequential Circuits for Low Power (J Monteiro et al.)

E 15 Embedded 'C' and RTOS

Embedded 'C': (25)

- Introduction to ANSI C, Basics of ANSI C, Control Structures: branching and looping, pointers, arrays, structures, unions, etc. (10)
- Keil Cx51 Compiler and compiler control directives. (3)
- Cx51 Language extensions: Keywords, memory types, memory models, data types, bit manipulation, etc. (4)
- Preprocessor and preprocessor directives. (3)
- Cx51 Compiler Library reference. (5)

RTOS: (30)

- Introduction to RTOS: Introduction, What is an RTOS, RTOS Scheduler, objects, services, Key characteristics of an RTOS. (4)
- Tasks: Introduction, Defining a task, task states and scheduling, task structures, synchronization, communication and concurrency. (4)
- Kernel objects: Semaphores, queues, pipes, event registers, signals, and condition variables. (3)
- Exceptions and interrupts: Introduction, Exception v/s Interrupt, Applications of exceptions and interrupts, (3)
- Timer and timer services: Introduction, Real-time clock and system clock, Programmable interval timers, Timer ISRs, Timing wheels, soft timers. (5)
- I/O subsystem: Basic I/O concepts, The I/O subsystem. (4)
- Memory Management: Introduction, Dynamic memory allocation in Embedded systems, Fixed-size memory allocation, blocking v/s non-blocking memory functions, H/W memory management units (5)
- Commercially available RTOS (PSOS, ThreadX, VXWorks, Nucleus, WinCE), Introduction to VxWorks (2)

Books: (Embedded 'C')

1. The C Programming Language, Second Edition, **Kernighan & Ritchie**, Prentice-Hall, Inc.
2. C: A Reference Manual, Second Edition, **Harbison & Steel**, Prentice-Hall Software Series
3. C and the 8051: Programming and Multitasking, **Schultz**, P T R Prentice-Hall, Inc.

Books: (RTOS)

1. Real-Time Concepts for Embedded Systems, Qing Li, Caroline Yao, CMP Books.
2. An Embedded Software Primer, David E. Simon, Addison-Wesley.
3. Patterns for Time-Triggered Embedded Systems: Building Reliable Applications with the 8051 Family of Microcontrollers (with CD-ROM), Michael J. Pont, Addison-Wesley
4. Embedded C (With CD-ROM), Michael J Pont, Addison-Wesley.
5. Embedded Systems Building Blocks: Complete and Ready-To-Use Modules in C, Jean J. Labrosse, CMP Books.
6. C Programming for Embedded Systems, Kirk Zurell, RD Books (CMP Books).

C 21 DSP Processors Fundamentals

Architecture and instruction set of DSP processor
Introduction to TMS320C6x processor, architecture, pipelining, linear and circular addressing modes, TMS320C6x instruction set, assembler directives, timers, interrupts, serial I/O, DMA, fixed and floating point data format,

Digital signal processing and DSP systems: Advantages of DSP, characteristics of DSP systems, DSP applications. DSP processors, architecture and instruction set.

Numeric representations and arithmetic: floating point numbers, IEEE 754 standard for floating point numbers,

Memory Architectures: memory structures, wait states, extended memory interfaces, addressing mechanisms.

Execution control: Hardware looping, interrupts, stack, relative branch support.

Pipelining: pipelining and performance, pipelining depth, interlocking, branching effects, interrupt effects, ;

Peripherals: serial / parallel ports, timers, communication ports, on-chip A^D and D/A converters,- external interrupts, on-chip debugging facilities, power consumption, clocking.

Books:

1. DSP Processor Fundamentals: architectures and Features, by Phil Lapsley, Wiley
2. DSP Applications using C and the TMS320C6x DSP

C 22 High Speed Digital Design Techniques

Unit 1: High Speed ADCs

Fundamental of high speed sampling, Base band antialiasing filters, Study of Harmonic sampling and bandpass sampling, Direct IF to digital conversion, Distortion and noise in an ideal N bit ADC, AD9220 12 bit ADC, Spurious free Dynamic Range, Measurement of Noise Power Ratio, Flash converters, Case study of AD9066, Study of latency of ADCs,

Unit 2: High Speed ADC Applications

Driving ADC inputs for low distortion and wide dynamic range, Applications of high speed ADCs in CCD imaging, High speed ADC applications in Digital transceivers

Unit 3: High Speed DACs and DDS Systems

Introduction to DDS, Aliasing in DDS Systems, 125 MSPS DDS System case study AD9850, DDS systems as ADC Clock Drivers, Amplitude modulation in a DDS System, The AD9831 Complete DDS System, High Speed low distortion DAC architecture, High Speed interpolating DACs, QPSK signal generation using DDS

Unit 4: Design issues of high speed Electronics

Simulation tools, Prototyping Circuits, Grounding in high speed systems, Power supply noise reduction and filtering, Power supply conditioning, EMI/RFI considerations, Shielding concepts

Reference Books:

1. High-Speed Digital Design: A Handbook of Black Magic by Howard Johnson
2. High Speed Signal Propagation: Advanced Black Magic by Howard W. Johnson
3. Signal Integrity Issues and Printed Circuit Board Design by Douglas Brooks
4. High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices by Stephen H. Hall
5. Signal Integrity - Simplified by Eric Bogatin
6. Handbook of Digital Techniques for High-Speed Design : Design Examples, Signaling and Memory Technologies, Fiber Optics, Modeling, and Simulation to Ensure ... (Prentice Hall Modern Semiconductor Design) by Tom Granberg
7. Noise Reduction Techniques in Electronic Systems, 2nd Edition by Henry Ott
8. High Speed Design Techniques, Manual by analog Devices, October 1996

C 23 Advanced Computer

Networks Unitl:Ipv6
Advanced IPv6 features, including transition. Mobile IPv6 operation. Models to support (WLAN) network roaming , IPv6 transition methods ;

Unit 2: Network Security
Advanced IP routing and multihoming, Challenging networking scenarios. Advanced security issues ' ^'"^y^'"^ Network performance and monitoring. Advanced IP Multicast

Unit 3: Configuring the Network:
Link-local and Adminstrator-less networking. Topics in Dynamic Host Configuration, Node and Service Discovery, Multi-homing in Enterprise networks. Issues with renumbering live networks

Unit 4: TCP/IP and Wireless communication technologies:
TCP/IP fundamentals, TCP/IP network simulations, TCP/IP modeling
Reviews on wireless communication technologies, WLAN, Bluetooth, TCP/IP over Wireless Networks

Unit 5: P2P and Overlay Network:
Routing, Multicast, Content Distribution Networks, Content addressing, search, and retrieval

Unit 4: Different type of advanced networks
Bluetooth, 802.11. HiperLAN2, **GPRS** and Edge Services, UMTS, **3G,** Beyond **3G:** integrated **4G** services. Access technologies: last mile, xDSL, Reviews of packet switching

Unit 5: Advanced topics in Computer Networking
Multimedia over a Network, Streaming over Internet, Streaming over wired and wireless Network, Wireless Sensor Networks, Wireless Home Networks

Reference Books

1. Computer Networking: A Top-Down Approach Featuring the Internet, by James Kwose and Keith Ross, ISBN: 0-201-97699-4, Addison-Wesley, 2/e, 2002
2. IP SANS: A Guide to iSCSI, iFCP, and FCIP Protocols for Storage Area Networks, by Thomas dark, ISBN: 0-201-75277-8, Addison-Wesley, 2002
3. Storage Area Network Fundamentals, by Meeta Gupta, ISBN: I-58705-065-X, Prentice Hall, April 2002 ^ :;.-
4. Designing Storage Area Networks: A Practical Reference for Implementing Fibre Channel and IP SANs, 2/E, by Tom dark, ISBN: 0-321-13650-0, Addison-Wesley, 2003
5. Wireless Communications and Networks, by William Stallings, ISBN: 0-13-040864-6, Prentice Hall, 2002
6. Computer Networks: A Systems Approach, 2/e, by Lan-y Peterson and Bruce Davie, ISBN: 1-55860-514-2, Morgan Kaufinann Publishers, 2000

E 24 (V) Microelectromechanical Systems

History of MicroElectroMechanical Systems (MEMS), market for MEMS, basics of microtechnology, lithography and etching techniques, principles of bulk and surface micromachining: subtractive processes, additive processes (evaporation, sputtering, epitaxial growth). Fundamental devices and processes, Multi User MEMS Process (MUMPs), SUMMiT: design rules; applications; micro hinges and deployment actuators, CMOS MEMS, cleanroom lab techniques, MicroOptoElectroMechanical Systems (MOEMS), bioMEMS and biomaterials, piezoresistivity; scanning probe microscopy, scaling laws, applications.

Lumped element modeling and design, Electrostatic Actuators , Electromagnetic Actuators, Linear and nonlinear system dynamics, resonant systems, Elasticity (stress, strain, material properties), Mechanical structure basics (bending of beams, torsion,

natural frequency), Optical system design basics (Gaussian beam optics, matrix optics, resolution)

Application case studies: MEMS Scanners and Retinal Scanning Displays (RSD), Grating Light Valve (GLV), Digital Micromirror Devices (DMD), Optical switching, Capacitive Micromachined Ultrasonic Transducers (CMUT)

Reference Books:

1. Gregory T A 1998, Kovacs Micromachined Transducers Sourcebook, WCB McGraw-Hill.
2. Nadim Maluf, *An introduction to Microelectromechanical system design*, Artech House, 2000
3. Victor M. Bright, Editor, *Selected papers on Optical MEMS,* SPIE Milestone Series, Volume MS 153, SPIE Press, 1999
4. Mohamed Gad-el-Hak*,* Editor, *The MEMS Handbook*, CRC Press, Baco Raton, 2001
5. Marc Madou*, Fundamentals of Microfabrication*, CRC Press, New York, 1997.
6. Gregory T. A. Kovacs*, Micromachined Transducers Sourcebook*, WCB / McGraw-Hill
7. W. Trimmer, Editor, Micromechanics and MEMS: Classic and Seminal Papers to 1990, IEEE Press, 1996

E-24 (E) FPGA/CPLD Based Systems

Unit 1:
Introduction. Basic Concepts. Digital Design and FPGAs. FPGA-Based System Design. Summary. Problems.

Unit 2:
VLSI Technology behind FPGA/CPLD, Manufacturing Processes. CMOS Logic Gates. Wires, Registers and RAM, Packages and Pads

Unit 3:

FPGA Fabrics. FPGA Architectures. SRAM-Based FPGAs. Permanently Programmed FPGAs. Chip I/O. Circuit Design of FPGA Fabrics. Architecture of FPGA Fabrics.

Unit 4:

Combinational Logic, The Logic Design Process. Hardware Description Languages. Combinational Network Delay. Power and Energy Optimization. Arithmetic Logic. Logic Implementation for FPGAs. Physical Design for FPGAs. The Logic Design Process Revisited. Summary. Problems.

Unit 5:

Sequential Machines, The Sequential Machine Design Process. Sequential Design Styles. Rules for Clocking. Performance Analysis. Power Optimization.

Unit 6:

Architecture, Behavioral Design. Design Methodologies. Design Example. Summary. Problems.

Unit 7:

Large-Scale Systems. Busses. Platform FPGAs. Multi-FPGA Systems. Novel Architectures.

References:

1. FPGA-Based System Design Wayne Wolf, Verlag: Prentice Hall PTR
3. Modern VLSI Design: System-on-Chip Design (3rd Edition) (3RD) Wayne Wolf

E 25 DSP Algorithms and Applications

Algorithms: - Modern DSP algorithms for audio Video and multimedia.

Applications in Telecommunications: - A view of Telecommunication system, digital system, digital transmission, digital switching, digital signal processing in pulse code modulation and frequency division multiplex transmission terminals, Aliased harmonic distortion, echo control, consideration for digital processing hardware.

Audio signal processing: - Linear pulse code modulation, Floating point PCM, Delta modulation, Adaptive delta modulation, Recorders- Digital tape recorders, reverberations, reception and transduction, Measurement techniques.

Digital Processing of Speech: - Mode of speech waveform, Speech synthesis and short time Fourier analysis and synthesis of speech, synthesis by linear prediction, pole zero mode of speech.

Digital Image Processing: - Image formation and recording, Image sampling and quantization, Reconstruction and display of digital images, Properties of human visual system, Spatial domain image compression, Deblurring, Basic deblurring methods.

Books: -
1.Applications of DSP, Alan Oppenheim, John Wiley and Sons, New York.
2.VLSI signal processing systems, K.K Parthi.
3.Architechures for DSP, Peter Prissch, John Wiley and Sons, New York.

E25 (V) Computer Aids for VLSI Design

The Characteristics of Digital Electronic Design

Design, Hierarchy Views, Connectivity, Spatial Dimensionality, Design Environments, System Level, Algorithm Level, Component Level, Layout Level

Representation

General Issues of Representation, Hierarchy Representation, View Representation, Connectivity Representation, Geometry Representation

Synthesis Tools
Introduction, Cell Contents Generation and Manipulation, Generators of Layout Outside the Cells, Cells and Their Environment, Silicon Compilers, Postlayout Generators

Static Analysis Tools: Node Extraction, Geometrical Design-Rule Checkers, Electrical-Rule Checkers, Verification, Dynamic Analysis Tools
Circuit-Level Simulators, Logic-Level Simulators, Functional- and Behavioral-Level, Simulation Issues, Event-Driven Simulation, Hardware and Simulation

The Output of Design Aids: Circuit Boards, Integrated Circuits, Implementation Issues, Programmability, Imperative Programming, Declarative Programming, Hierarchy

Graphics Display Graphics, Hardcopy Graphics, Input Devices, Human Engineering, Task and User Modeling, Information Display, Command Language
And Feedback, Electric, Representation, Programmability, Environments, Tools
For Designing a Chip

Formats: Gerber Format, Caltech Intermediate Format, GDS II Format, Electronic Design Interchange Format, EBES Format

Reference Books:

1. Algorithms for VLSI Design Automation by Sabih H. Gerez, Wiley Publications
2. Computer Aids for VLSI Design, Second Edition, Steven M. Rubin
Silicon VLSI Technology: Fundamentals, Practice, and Modeling, James D. Plummer, Michael D. Deal, Peter B. Griffin.

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