## Course Structure and Scheme of Evaluation
### Semester I

<table>
<thead>
<tr>
<th>Course Code</th>
<th>Course</th>
<th>Teaching Scheme</th>
<th>Credits</th>
</tr>
</thead>
<tbody>
<tr>
<td>C 10</td>
<td>Research Methodology (Audit)</td>
<td>L 2 T - P -</td>
<td></td>
</tr>
<tr>
<td>C11</td>
<td>High Speed Analog Design</td>
<td>L 4 T - P -</td>
<td>4</td>
</tr>
<tr>
<td>C12</td>
<td>Reconfigurable Platforms &amp; HDL</td>
<td>L 4 T - P -</td>
<td>4</td>
</tr>
<tr>
<td>C 13</td>
<td>Communication Networks</td>
<td>L 4 T - P -</td>
<td>4</td>
</tr>
<tr>
<td>E 14</td>
<td>Elective-I</td>
<td>L 3 T - P -</td>
<td>3</td>
</tr>
<tr>
<td>E 15</td>
<td>Elective-II</td>
<td>L 3 T - P -</td>
<td>3</td>
</tr>
<tr>
<td>C 14</td>
<td>High Speed Analog Design Lab</td>
<td>L - T 2 P 1</td>
<td></td>
</tr>
<tr>
<td>C 15</td>
<td>Reconfigurable Platforms &amp; HDL Lab</td>
<td>L - T 2 P 1</td>
<td></td>
</tr>
<tr>
<td>C 16</td>
<td>Communication Networks Lab</td>
<td>L - T 2 P 1</td>
<td></td>
</tr>
<tr>
<td>S 16</td>
<td>Seminar –I</td>
<td>L - T 2 P 2</td>
<td></td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td></td>
<td>L 20 T 0 P 8</td>
<td>23</td>
</tr>
</tbody>
</table>

Total Contact hours per week = 28

### Elective - I
- E14(V) Memory Technologies
- E 14 (V) CMOS VLSI Design
- E14(E) Asynchronous Circuit Design
- E 14 (E) Advanced Computer Architecture

### Elective - II
- E15(V) Digital System And Testing
- E 15 (V) Mixed Signal ASIC Design
- E 15 (E) RISC Microcontrollers
- E 15 (E) Automotive Embedded Systems

Specialization: V VLSI Design
- E Embedded Systems

M.Tech Electronics Technology Syllabus w.e.f from Academic year 2012-2013
## Course Structure and Scheme of Evaluation
### Semester II

<table>
<thead>
<tr>
<th>Course Code</th>
<th>Course</th>
<th>Teaching Scheme</th>
<th>Credits</th>
</tr>
</thead>
<tbody>
<tr>
<td>C 21</td>
<td>DSP Processor</td>
<td>4 - - -</td>
<td>4</td>
</tr>
<tr>
<td>C 22</td>
<td>Real Time Operating System</td>
<td>4 - - -</td>
<td>4</td>
</tr>
<tr>
<td>C 23</td>
<td>High Speed Digital Design</td>
<td>4 - - -</td>
<td>4</td>
</tr>
<tr>
<td>E 24</td>
<td>Elective-III</td>
<td>3 - - -</td>
<td>3</td>
</tr>
<tr>
<td>E 25</td>
<td>Elective-IV</td>
<td>3 - - -</td>
<td>3</td>
</tr>
<tr>
<td>C 24</td>
<td>DSP Processor Lab</td>
<td>- - 2 -</td>
<td>2</td>
</tr>
<tr>
<td>C 25</td>
<td>Real Time Operating System Lab</td>
<td>- - 2 -</td>
<td>2</td>
</tr>
<tr>
<td>C 26</td>
<td>High Speed Digital Design Lab</td>
<td>- - 2 -</td>
<td>2</td>
</tr>
<tr>
<td>S 26</td>
<td>Seminar –II</td>
<td>- - 2 -</td>
<td>2</td>
</tr>
</tbody>
</table>

**Total** 18 0 8 23

Total Contact hours per week = 26

#### Elective – III

- E24(V) System on Chip
- E 24 (V) Wavelet Transform and Applications
- E24(E) MicroElctroMechanical System
- E 24 (E) Robotics and Machine Vision

#### Elective - IV

- E25(V) RF Integrated Circuit Design
- E 25 (V) VLSI in Signal Processing
- E25(E) High Performance Networks
- E 25 (E) Mobile Computing

Specialization : V VLSI Design
- E Embedded Sysems
Course Structure and Scheme of Evaluation
Semester III

<table>
<thead>
<tr>
<th>Course Code</th>
<th>Course</th>
<th>Teaching Scheme</th>
</tr>
</thead>
<tbody>
<tr>
<td>T 31</td>
<td>* Industrial Training</td>
<td>-   - 2</td>
</tr>
<tr>
<td>S 32</td>
<td>Dissertation Phase-I</td>
<td>-   - 5</td>
</tr>
<tr>
<td></td>
<td><strong>Total</strong></td>
<td>-   - 7</td>
</tr>
</tbody>
</table>

**Total Contact hours per week/students = 2 & 5 respectively for T31 & S32

8 Weeks at the end of First Year (Summer)

** Average contact hours/week/student

Course Structure and Scheme of Evaluation
Semester IV

<table>
<thead>
<tr>
<th>Course Code</th>
<th>Course</th>
<th>Teaching Scheme</th>
</tr>
</thead>
<tbody>
<tr>
<td>D 42</td>
<td>Dissertation Phase-II</td>
<td>-   - 5</td>
</tr>
<tr>
<td></td>
<td><strong>Total</strong></td>
<td>-   - 5</td>
</tr>
</tbody>
</table>

Total Contact hours per week = 5
SHIVAJI UNIVERSITY
M.TECH (Electronics Technology) PROGRAMMES

Semester I

C-10 Research Methodology

Teaching Scheme
Examination Scheme

Lectures: 2 Hrs./Week

Unit 1 Research Methodology: An Introduction
Objectives of Research, Types of Research, Research Methods and Methodology, Defining a Research Problem, Techniques involved in Defining a Problem

Unit 2 Research Design

Unit 3 Measurement and Scaling Techniques
Measurement in Research, Measurement Scales, Scales, Sources in Error, Techniques of Developing Measurement Tools, Scaling, Meaning of Scale, Scale Construction Techniques

Unit 4 Methods of Data Collection and Analysis
Collection of Primary and Secondary Data, Selection of appropriate method, Data Processing Operations, Elements of Analysis, Statistics in Research, Measures of Dispersion, Measures of Skewness, Regression Analysis, Correlation

Unit 5 Techniques of Hypotheses, Parametric or Standard Tests
Basic concepts, Tests for Hypotheses I and II, Important parameters, Limitations of the tests of Hypotheses, Chi-square Test, Comparing Variance, as a non-parametric Test, Conversion of Chi to Phi, Caution in Using Chi-square test

Unit 6 Analysis of Variance and Co-variance
ANOVA, One way ANOVA, Two Way ANOVA, ANOCOVA, Assumptions in ANOCOVA, Multivariate Analysis Technique, Classification of Multivariate Analysis, factor Analysis, R-type Q Type Factor Analysis, Path Analysis

Interpretation and Report

M.Tech Electronics Technology Syllabus w.e.f from Academic year 2012-2013
M.TECH (Electronics Technology) PROGRAMMES

Semester I

C 11 High Speed Analog Design Techniques

Teaching Scheme

Lectures: 4 Hrs./Week
Credit: 4
Practical: 2 Hrs/Week
Credit: 1

Unit 1: High Speed Operational Amplifiers

Unit 2: High-Speed applications based on Op-amps
Optimizing feedback network for maximum bandwidth fitness, Driving Capacitive load, Cable drivers and receivers, High performance video line driver, Differential line drivers and receivers, High speed clamping amplifiers, High speed current to voltage converters and the effects of inverting input capacitance,

Unit 3: High speed amplifiers for communication applications
Low noise amplifiers for communication systems, Mixers, Power amplifiers, Liner drivers, Automatic gain control amplifiers

Unit 4: High speed system for video applications
High speed video multiplexing with Opamps using disable function, Video programmable gain amplifier, Video multiplexers and Cross Point switches, High power line drivers and ADSL, High speed photodiode Pre amps, Case studies of AD830, AD9002

Unit 5: High speed RF/IF Subsystems
Dynamic range compression, Linear VCAs, Log/Limiting Amplifiers, Receiver overview, Multipliers, modulators and mixers,

Unit 6:
Case study of AD600 Dual Channel X-amp, AD641 monolithic log amplifier.

Reference Books:

M.Tech Electronics Technology Syllabus w.e.f from Academic year 2012-2013
Semester I
C 12 Reconfigurable Platforms and HDL

Teaching Scheme

Examination Scheme

Lectures: 4 Hrs./Week
Credit: 4
Practical: 2 Hrs/week
Credit: 1

Unit 1:
Computing requirements, Area, Technology scaling, Instructions, Custom Computing Machine, Overview, Comparison of Computing Machines.

Unit 2:
Interconnects, Requirements, Delays in VLSI Structures; Partitioning and Placement, Routing; Computing Elements, LUT’s, LUT Mapping, ALU and CLB’s, Retiming, Fine-grained & Coarse-grained structures; Multicontext; Comparison of different architectures viz. PDSPs, RALU, VLIW, Vector Processors, Memories.

Unit 3:
Arrays for fast computations, CPLDs, FPGAs, Multicontext, Partial Reconfigurable Devices; TSFPGA, DPGA, Matrix; Best suitable approach for RD; Case study. Control Logic, Binding Time and Programming Styles, Overheads, Data Density, Data BW, Function density, Function diversity, Interconnect methods, Best suitable methods for RD;

Unit 4:
Contexts, Context switching; Area calculations for PE; Efficiency, ISP, Hot Reconfiguration; Case study. Architectures for existing multi FPGA systems, Compilation Techniques for mapping applications described in a HDL to reconfigurable hardware, Study of existing reconfigurable computing systems to identify existing system limitations and to highlight opportunities for research;

Unit 5:
Software challenges in System on chip; Testability challenges; Case studies. Modeling, Temporal portioning algorithms, Online temporal placement, Device space management.

Unit 6:
Direct communication, Third party communication, Bus based communication, Circuit switching, Network on chip, Dynamic network on chip, Partial reconfigurable design.
References:
1. Andre Dehon, “Reconfigurable Architectures for General Purpose Computing”.
2. IEEE Journal papers on Reconfigurable Architectures.
M.Tech Electronics Technology Syllabus w.e.f from Academic year 2012-2013
SHIVAJI UNIVERSITY
M.TECH (Electronics Technology) PROGRAMMES

Semester I
C 14 High Speed Analog Design Lab

Practical : 2 hrs./week
Credit : 1

Students are instructed to frame and perform laboratory assignments, based on each of the theory course. The assignment should encompass the hardware techniques and software tools introduced in the concerned subjects and should prove to be useful for the PG programs in the relevant discipline. Assignment should be a full-fledged system design type problem with multi-dimensional solutions suggested. Assignment should be implemented using known hardware techniques/software tools and should be reliably executable.

Student shall submit a laboratory work document based on these assignments performed at the end of semester. The Laboratory instructor shall guide the students in framing the assignments and defining the problem pertaining to the said subjects.
C 15  Reconfigurable Platforms & HDL Lab

Practical : 2 hrs./week
Credit : 1

Students are instructed to frame and perform laboratory assignments, based on each of theory course. The assignment should encompass the hardware techniques and software tools introduced in the concerned subjects and should prove to be useful for the PG programs in the relevant discipline. Assignment should be a full-fledged system design type problem with multi-dimensional solutions suggested. Assignment should be implemented using known hardware techniques/software tools and should be reliably executable. Student shall submit a laboratory work document based on these assignments performed at the end of semester. The Laboratory instructor shall guide the students in framing the assignments and defining the problem pertaining to the said subjects.
SHIVAJI UNIVERSITY
M.TECH (Electronics Technology) PROGRAMMES
Semester I

C 16  Communication Network  Lab

Practical : 2 hrs./week       Credit : 1

Students are instructed to frame and perform laboratory assignments, based on each of theory course. The assignment should encompass the hardware techniques and software tools introduced in the concerned subjects and should prove to be useful for the PG programs in the relevant discipline. Assignment should be a full-fledged system design type problem with multi-dimensional solutions suggested. Assignment should be implemented using known hardware techniques/software tools and should be reliably executable.

Student shall submit a laboratory work document based on these assignments performed at the end of semester. The Laboratory instructor shall guide the students in framing the assignments and defining the problem pertaining to the said subjects.
SHIVAJI UNIVERSITY
M.TECH (Electronics Technology) PROGRAMMES

Semester I

ELECTIVE-I

E14 (V) Memory Technologies

Teaching Scheme

Examination Scheme

Lectures: 3 Hrs./Week
Credit: 3

Unit 1
Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, SOI, Advanced SRAM Architectures, Application Specific SRAMs;

Unit 2
DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAM,

Unit 3
High Density ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Nonvolatile SRAM, Flash Memories. RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory

Unit 4

Unit 5
Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing, Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices.

Unit 6
Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging, Future Directions, Introduction to digital tablet PC, LCD, DVD player etc.

References:

M.Tech Electronics Technology Syllabus w.e.f from Academic year 2012-2013
SHIVAJI UNIVERSITY
M.TECH (Electronics Technology) PROGRAMMES

Semester I

E14 (V) CMOS VLSI Design

Teaching Scheme
Examination Scheme
Lectures: 3 Hrs./Week
Credit: 3

Unit 1: Basics of CMOS
VLSI Design: History, Trends, Principles, Metrics, CMOS transistors (n-channel and p-channel), The CMOS Switch model, CMOS Inverter mode, Logic devices and interconnect, CMOS circuit analysis: transistors, inverters, interconnect modeling, parasitics, CMOS Process and Layout, CMOS Devices: SPICE and deep sub-micron issues 6hrs.

Unit 2: CMOS: Design Issues
CMOS Inverter: speed, power and scaling, Static CMOS Gates, Dynamic CMOS Gates, Power Estimation and Optimization 7hrs.

Unit 3: Modeling

Unit 4: Circuits to Systems
VLSI circuits to systems, Circuit modeling and layout (demo using standard tools), CMOS design and layout tools, Nano-electronics circuits versus CMOS microelectronics circuits, Nano-computing techniques and device platforms 7hrs.

Unit 5: Digital IC Design

Unit 6: Timing issues for Digital CMOS circuits
Timing Issues, Clock skew, clocking styles, Self-timed circuit design, Case study of Kitchen timer chip 7hrs.

Reference Books:
3. Weste and Harris, CMOS VLSI Design, a Circuits and Systems Perspective (3rd edition)
E 14 (E) Asynchronous Circuit Design

Teaching Scheme

Lectures: 3 Hrs./Week
Credit: 3

Unit 1.
Introduction to asynchronous circuit design, Communication channels, Modeling asynchronous communication in VHDL, Example: MiniMIPS

Unit 2.
Communication protocols, Handshaking expansion, Data Encoding, Syntax-directed translation, Graphical representations, Asynchronous finite state machines, Petri nets, Timed event/level structures

Unit 3
Huffman circuits, Solving covering problems, State minimization, State assignment, Hazard-free logic synthesis, Extensions for MIC operation

Unit 4.
Muller circuits, Complete state coding Hazard-free logic synthesis, Hazard-free decomposition

Unit 5
Timing circuits, Zones, POSET Timing, Verification, Circuit verification, Protocol verification

Unit 6.
Applications, History/RAPPID, Performance analysis/testing, Synchronization problem

References Book:
“Asynchronous Circuit Design”, Chris J. Myers, John Wiley & Sons, Inc
E 14 (E) Advanced Computer Architecture

Teaching Scheme
Lectures: 3 Hrs./Week
Credit: 3

UNIT 1 INSTRUCTION LEVEL PARALLELISM
6hrs.
ILP – Concepts and challenges – Hardware and software approaches – Dynamic scheduling – Speculation - Compiler techniques for exposing ILP – Branch prediction.

UNIT 2 MULTIPLE ISSUE PROCESSORS
7hrs.
VLIW & EPIC – Advanced compiler support – Hardware support for exposing parallelism – Hardware versus software speculation mechanisms – IA 64 and Itanium processors – Limits on ILP.

UNIT 3 MULTIPROCESSORS AND THREAD LEVEL PARALLELISM
6hrs.

UNIT 4 MEMORY AND I/O
7hrs.

UNIT 5 MULTI-CORE ARCHITECTURES
6hrs.
Software and hardware multithreading – SMT and CMP architectures – Design issues –


7hrs.
TEXT BOOKS:

REFERENCES:
SHIVAJI UNIVERSITY
M.TECH (Electronics Technology) PROGRAMMES
Semester I

Elective –II

E 15 (V) Digital Systems and Testing

Teaching Scheme

Examination Scheme

Lectures: 3 Hrs./Week
Credit: 3

Unit 1: Testing
Testing Defined: definitions and areas within testing. Logic and Fault Modeling.
Mechanics

Unit 2: System life, Sources of defects?
Representation and models of digital systems across abstraction levels.
Fault Models: logical versus physical; SSL model, opens and shorts, bridging faults; Basic assumptions.
Review of minimization tools and asynchronous machines, Test Pattern Generation basics. (activate and drive.), Algebraic approaches, Fault Equivalence and Dominance.

Unit 3: Test Generation
Algebraic Approaches and Structural Approaches, Logic Simulation.
Algebraic Approaches: Boolean difference, Literal position, Effect of fanout on circuits, Checkpoint faults.
Structural Approaches to test generation. Path sensitization methods. Test Coverage

Unit 4: Logic simulations
Simulation engines: compiler, event driven. Representation of value, circuit, etc.

Unit 5: More Test Generation and D-algorithm
D-algorithm representation, cube algebra, generalized algorithm, Extensions to D-algorithm PODEM, FAN, etc. Random test generation, Complexity issues Functional Test Generation Methods, Heuristic Methods, Exhaustive and Pseudo Exhaustive techniques, RAM and PLA testing, Microprocessor testing, Memory Testing: Memory test complexity, Memory fault models.

Unit 6: Design for Testability
Controllability and Observability measures, STEFAN, Ad Hoc techniques, More Design for Testability, Scan Design. Scan Designs: IEEE Standards, Board-Level Testing: Boundary Scan, Data Compression and BIST, LFSR polynomial generation Data compression techniques Aliasing Probability, BIST, Self Checking and PLD Testing
References:

3. "HDL Chip Design" by Douglas Smith, Doone Publications, AL.
Teaching Scheme
Lectures: 3 Hrs./Week
Credit: 3

Unit 1: Technology and modeling aspects of an advanced BiCMOS ASIC process
LSI Logic analogue BiMOS technology, Background, Process technology, Well formation, Island definition and field region implants, Field oxidation - Island formation, High performance operational amplifiers and comparators
High performance amplifiers, The load compensated OTA (LC-OTA), The Miller compensated OTA (M-OTA), The core-amplifier (C-OTA), High performance comparators, The OTA as comparator, Latched comparators, A high speed accurate comparator.

Unit 2: Switched current techniques for analogue sampled data signal processing
Introduction, First generation memory cells, Second generation memory cells, Limitations of the basic SI memory cell, Channel length modulation, Charge injection, Junction leakage
Applications: Integrator based biquad, FIR filters, Sigma-Delta modulators

Unit 3: Data converters
Parameters for data converter characterisation, Data converters: Basic design considerations, High speed data conversion techniques, Current switched D/A converters, Flash and two-step flash converters, Limits to speed and resolution in data converters Oversampling converters, Intuitive Introduction to Oversampling Data Converters, Noise shaping converters, First order sigma delta modulators Second order sigma delta modulator, Multistage sigma-delta modulator, Non ideal effects in sigma delta modulators, Sampling jitter

Unit 4: Self-calibrating and algorithmic converters
Self-calibrated analogue-digital converters, Architecture with segmented binary-weighted capacitor Array, Self-calibration technique and circuits, Principle of calibration, Calibrating capacitors, Calibrating registers

Unit 5: A high flexibility BiCMOS standard cell library for mixed analogue-digital ASICs
A BiCMOS process dedicated to mixed A/D applications, Cell libraries, Analogue libraries, The digital cell library, CAD tools, The CAD capability, Telescopic Cells, Parametrisable cells, Adjustable cells, Automatic cell biasing and power down, ADS (Analog Design System) An environment for Mixed signal design, Analogue/digital multi-level mixed mode simulations, Case Studies:
Example 1: Infra red receiver with decoder and actuator Example 2: Remote control

Unit 6: Advanced topics:
Element matching, Local process variations, Global process variations, Process gradients, Boundary effects, Noise coupling, Substrate noise coupling, Signal noise coupling, Examples of optimized structures, Few applications of mixed signal ASICs:
Applications areas: A heart rate meter, Hearing aid ASIC, Sound and rhythm generator, TV picture in picture processor, A multi-standard modem, A speech scrambler de-scrambler.

M.Tech Electronics Technology Syllabus w.e.f from Academic year 2012-2013
References:

1. Analogue-digital ASICs: circuit techniques, design tools and applications, Edited by R.S. Soin, F. Maloberti and J. Franca, IEE Publications
2. Signal Integrity Effects in Custom IC and ASIC Designs, Raminderpal Singh (Editor), Wiley Publications
Teaching Scheme
Lectures: 3 Hrs./Week
Credit: 3

Unit- 1 PIC: Modern Architectures:
• Introduction: PIC microcontroller features, MPLAB IDE, PICmicro Architecture, Program memory, Instruction set, Instruction Format, Byte-Oriented Instructions, Bit-Oriented Instructions, Literal Instructions, Control Instructions (CALL and GOTO), Destination Designator (d), Addressing Modes

Unit- 2
• PIC micro Hardware: reset, clock, control registers, register banks, program memory paging, Ports, interrupts, Timer and Counter, watchdog timer, power up timer, sleep mode, state machine programming,

• MPLAB overview: Using MPLAB, Toolbars, Select Development Mode And Device Type, Project, Text Editor, Assembler, MPLAB Operations.

ARM :

Unit – 3

Unit – 4
ARM Embedded System, ARM Processor Fundamentals: Registers, Pipeline, Exceptions, Interrupts and vector tables, ARM Processor family, ARM Instruction Set, Thumb Instruction Set. Overview of C compiler and Optimization: Register allocation, Functions Calls, Pointer aliasing, Structure arrangement, Portability issues, writing and optimizing ARM assembly code

Unit – 5
Interrupts and interrupt handling Scheme, firmware and Boot loader, Real-Time operating Systems: Context Switching, task tables and kernels, Time Slice, Scheduler algorithms: RMS, Deadline monotonic Scheduling; Priority Inversion, Tasks, Threads and process, Exceptions, Exception handling

Unit – 6
Introduction to DSP on ARM –FIR Filter – IIR Filter – Discrete fourier transform – Exception Handling – Interrupts – Interrupt handling schemes- Firmware and bootloader

Books: (PIC)
SHIVAJI UNIVERSITY
M.TECH (Electronics Technology) PROGRAMMES

2. Embedded Design with the PIC18F452, John B. Peatman,
3. Programming & Customizing PICmicro Microcontrollers, MykePredko, TMH.
4. PIC in Practice, David W Smith, Newnes.
5. PIC Microcontroller: An Introduction to Software & Hardware Interfacing, Han-Way Huang, Thomson.

ARM

Text books:
1. Embedded Systems Architecture by Tammy Overgaard; Elsevier Publisher; 2005
2. ARM System Developer’s Guide by A.N. Sloss, D. Symes and C. Wright; Elsevier Publisher; 2006

Reference books:
1. Embedded System Design by Steve Heath, Elsveir Publisher; 2006
2. Embedded Systems by Raj Kamal, TMH; 2006
3. Embedded Microcomputer Systems, Thomson Publisher; 2005
4. Embedded system Design, Kluwer Academic Publisher; 2005
5. An Introduction to the design of small-scale embedded Systems by T. Wilmshurst, Palgrav publisher; 2001
E15 (E) AUTOMOTIVE EMBEDDED SYSTEMS

Teaching Scheme
Lectures: 3 Hrs./Week
Credit: 3

Unit 1
Current trends in Automobiles, open loop and closed loop systems - components for electronic engine management system. Electro magnetic interference suppression. Electromagnetic compatibility, Electronic dashboard instruments, onboard diagnostic system ,

Unit 2
security and warmingsystem. Electronic management of chassis systems.Vehicle motion control.Sensors and actuators, and their interfacing. Basic sensor arrangement, types of sensors such as oxygen sensors, crankangle position sensors- Fuel metering/ vehicle speed sensors and destination sensors, Attitude sensor,Flow sensor, exhaust temperature, air mass flow sensors. Throttle position sensor

Unit 3
solenoids, stepper motors, relays. Electronic ignition systems. Types of solid state ignition systems and their principle of operation.

Unit 4
Digital engine control system. Open loop and closed loop control system, Engine cranking and warm up control. Acceleration enrichment. Deceleration learning and ideal speed control, Distributor less ignition – Integrated engine control system, Exhaust emission control engineering.

Unit 5
Automotive Embedded systems.
PIC, Freescale microcontroller based system. Recent advances like GLS, GPSS, GMS. Multiprocessor communication using CAN bus.

Unit 6
Case study- cruise control of car. Artificial Intelligence and engine management

References:

M.Tech Electronics Technology Syllabus w.e.f from Academic year 2012-2013
Teaching Scheme
Examination Scheme
Lectures: 4 Hrs./Week
Credit: 4
Practical: 2 Hrs/week
Credit: 1

Unit 1:
Architecture and instruction set of DSP processor
Introduction to TMS320C6x processor, architecture, pipelining, linear and circular addressing modes, TMS320C6x instruction set, assembler directives, timers, interrupts, serial I/O, DMA, fixed and floating point data format,

Unit 2:
Digital signal processing and DSP systems: Advantages of DSP, characteristics of DSP systems, DSP applications. DSP processors, architecture and instruction set.

Unit 3:
Numeric representations and arithmetic: floating point numbers, IEEE 754 standard for floating point numbers,

Unit 4:
Memory Architectures: memory structures, wait states, extended memory interfaces, addressing mechanisms.

Unit 5:
Execution control: Hardware looping, interrupts, stack, relative branch support
Pipelining: pipelining and performance, pipelining depth, interlocking, branching effects, interrupt effects,

Unit 6:
Peripherals: serial / parallel ports, timers, communication ports, on-chip A^D and D/A converters, external interrupts, on-chip debugging facilities, power consumption, clocking.

Books:
1. DSP Processor Fundamentals: architectures and Features, by Phil Lapsley, Wiley
2. DSP Applications using C and the TMS320C6x DSP
Semester II
C22 REAL TIME OPERATING SYSTEMS

Teaching Scheme
Examination Scheme
Lectures: 4 Hrs./Week
Credit: 4
Practical: 2 Hrs/week
Credit: 1

Unit 1:
6hrs.

Unit 2:
7hrs.

Unit 3:
6hrs.

Unit 4:
7hrs.

Unit 5:
6hrs.

Unit 6:
7hrs.

References:
1. μC/OS-II, The real time Kernel, Jean J. Labrosse, Lawrence: R & D Publications.

M.Tech Electronics Technology Syllabus w.e.f from Academic year 2012-2013
C 23 High Speed Digital Design

Teaching Scheme
Lectures: 4 Hrs. /Week
Credit: 4
Practical: 2 Hrs./Week
Credit: 1

Unit 1: High Speed ADCs
Fundamental of high speed sampling, Base band antialiasing filters, Study of Harmonic sampling and band pass sampling, Direct IF to digital conversion, Distortion and noise in an ideal N bit ADC, AD9220 12 bit ADC, Spurious free Dynamic Range, Measurement of Noise Power Ratio, Flash converters, Case study of AD9066, Study of latency of ADCs.

Unit 2: High Speed ADC Applications
Driving ADC inputs for low distortion and wide dynamic range, Applications of high speed ADCs in CCD imaging, High speed ADC applications in Digital transceivers.

Unit 3: High Speed DACs and DDS Systems
Introduction to DDS, Aliasing in DDS Systems, 125 MSPS DDS System case study AD9850, DDS systems as ADC Clock Drivers.

Unit 4:
Amplitude modulation in a DDS System, The AD9831 Complete DDS System, High Speed low distortion DAC architecture, High Speed interpolating DACs, QPSK signal generation using DDS.

Unit 5: Design issues of high speed Electronics
Simulation tools, Prototyping Circuits, Grounding in high speed systems.

Unit 6:
Power supply noise reduction and filtering, Power supply conditioning, EMI/RFI considerations, Shielding concepts.

Reference Books:
3. Signal Integrity Issues and Printed Circuit Board Design by Douglas Brooks
5. Signal Integrity - Simplified by Eric Bogatin
6. Handbook of Digital Techniques for High-Speed Design : Design Examples, Signaling and Memory Technologies, Fiber Optics, Modeling, and Simulation to Ensure ... (Prentice Hall Modern Semiconductor Design) by Tom Granberg

M.Tech Electronics Technology Syllabus w.e.f from Academic year 2012-2013
Semester II

C 24 DSP Processor Lab

Practical: 2 hrs./week  Credit: 1

Students are instructed to frame and perform laboratory assignments, based on each of theory course. The assignment should encompass the hardware techniques and software tools introduced in the concerned subjects and should prove to be useful for the PG programs in the relevant discipline. Assignment should be a full-fledged system design type problem with multi-dimensional solutions suggested. Assignment should be implemented using known hardware techniques/software tools and should be reliably executable. Student shall submit a laboratory work document based on these assignments performed at the end of semester. The Laboratory instructor shall guide the students in framing the assignments and defining the problem pertaining to the said subjects.
C 25 Real Time Operating System Lab

Practical : 2 hrs./week

Credit : 1

Students are instructed to frame and perform laboratory assignments, based on each of the theory course. The assignment should encompass the hardware techniques and software tools introduced in the concerned subjects and should prove to be useful for the PG programs in the relevant discipline. Assignment should be a full-fledged system design type problem with multi-dimensional solutions suggested. Assignment should be implemented using known hardware techniques/software tools and should be reliably executable.

Student shall submit a laboratory work document based on these assignments performed at the end of semester. The Laboratory instructor shall guide the students in framing the assignments and defining the problem pertaining to the said subjects.
Practical: 2 hrs./week
Credit: 1

Students are instructed to frame and perform laboratory assignments, based on each of theory course. The assignment should encompass the hardware techniques and software tools introduced in the concerned subjects and should prove to be useful for the PG programs in the relevant discipline. Assignment should be a full-fledged system design type problem with multi-dimensional solutions suggested. Assignment should be implemented using known hardware techniques/software tools and should be reliably executable. Student shall submit a term-work document based on these assignments performed at the end of semester. The Laboratory instructor shall guide the students in framing the assignments and defining the problem pertaining to the said subjects.
Semester II

Elective-I

E 24 (V) Systems on Chip

Teaching Scheme

Lectures: 3 Hrs./Week  
Credit: 3

Unit 1:
IC Technology, Economics, CMOS Technology overview, Power consumption, Hierarchical design, Design Abstraction, EDA tools. 6hrs.

Unit 2:
MOSFET model, parasitics, latch up, advanced transistor structures; Wire parasitics; Design rules, Scalable design rules, process parameters; stick diagrams, Layout design tools; Layout synthesis, layout analysis. 7hrs.

Unit 3:
CMOS gate delays, transmission time, speed power product, low power gates; Delay by RC trees, cross talk, RLC delay, cell based layout, Logic & interconnect design, delay modeling, wire sizing; Power optimization, Switch logic networks. 6hrs.

Unit 4:
Pipelining, Data paths, Adders, ALUs, Multipliers, High density memories; Metastability, Multiphase clocking; Power optimization, Design validation, Sequential testing; Architecture for low power. 7hrs.

Unit 5:
Floor planning methods, global routing, switch box routing, clock distribution; off chip connections, packages, I/O architectures, pad design. 6hrs.

Unit 6:
Complete chip design including architecture, logic and layout for Kitchen timer chip OR Microwave oven chip. 7hrs.

Reference books:

Semester II

E 24 (V) Wavelet Transform and its applications

Teaching Scheme
Examination Scheme
Lectures: 3 Hrs./Week
Credit: 3

Unit 1. Continuous wavelet Transform
Introduction, Continuous-Time Wavelets, Definition of the CWT, The CWT as a Correlation. Constant Q-Factor Filtering Interpretation and Time-Frequency resolution, The CWT as an Operator, Inverse CWT.

Unit 2. Introduction to the Discrete Wavelet Transform and Orthogonal-Wavelet Decomposition
Introduction, Approximation of Vectors in Nested Linear Vector Subspaces,
(i) Example of Approximating Vectors in Nested Subspaces of a Finite-Dimensional Linear Vectors Space,
(ii) Example of Approximating Vectors in Nested Subspaces of an infinite-Dimensional Linear Vectors space,
Example of an MRA, (i) Bases for the Approximation subspaces and Haar Scaling function,
(ii) Bases for the Detail Subspaces and Haar Wavelet,
(iii) Digital Filter Implementation of the Haar Wavelet Decomposition.

Unit 3. NIRA, Orthonormal-Wavelets, and their Relationship to Filter Banks
Introduction, Formal Definition of an MRA, Construction of a General Orthonormal MRA,
(i) Scaling Function and Subspaces,
(ii) Implication of the Dilation Equation and Orthogonality,
A wavelet Basis for the MRA
(i) Two scale Relation for \( t \),
(ii) Basis for the detail subspaces
(iii) Direct sum decomposition,
Digital Filtering interpretation.
(i) Decomposition Filters,
(ii) Reconstructing the Signal.
Examples of Orthogonal Basis-Generating Wavelets,
(i) Daubechies D4 Scaling Function and Wavelet,
(ii) Band limited Wavelets, Interpreting Orthonormal MRAs for 40 Discrete-Time Signals,
(i) Continuous-Time MRA interpretation for DTWT,
(ii) Discrete-Time MRA,
(iii) Basis Functions for the DTWT, Miscellaneous issues related to PRQMF Filter Banks, Generating Scaling Functions and Wavelets from Filter Coefficients
Unit 4. Alternative Wavelet Representations

Introduction, Biorthogonal Wavelet Bases, Filtering Relationship for Biorthogonal Filters, Examples of Biorthogonal Scaling Functions and Wavelets, Two-Dimensional Wavelets, Nonseparable Multidimensional Wavelets, Wavelet packets.

Unit 5. Wavelet Transform and Data Compression

Introduction, Transform coding, DTWT for Image Compression,
(i) Image Compression using DTWT and Run-Length Encoding,
(ii) Embedded Tree Image Coding,
(iii) Comparison with JPEG, Audio Compression.
(I) Audio Masking,
(ii) Standards Specifying Subband Implementation: ISO/MPEG Coding for Audio,
(iii) Wavelet-Based Audio Coding, Video Coding Using Multiresolution Techniques: A Brief Introduction.

Unit 6. Other Applications of Wavelet Transforms

Introduction, Wavelet Denoising, Speckle Removal, Edge Detection and Object Isolation, Image Fusion, Object Detection by Wavelet Transforms of Projections, Communication Applications,
(i) Scaling Functions as Signaling Pulses,
(ii) Discrete Wavelet Multitone Modulation

1. Text Book:

2. Reference Book:
   1. Wavelets and Filter Banks, Gilbert Stang & Truong Nguyen-Wellesly -1996

References:
1. P. P. Vaidyanathan: Multirate Systems & Filter Banks, PTR, PH, 19932.
2. Gilbert Strang: Linear Algebra and its Applications.
5. Strang G S, T Q Nguyen: Wavelets and Filter Banks,
M.TECH (Electronics Technology) PROGRAMMES

Semester II

E 24 (E) Microelectromechanical Systems

Teaching Scheme

Examination Scheme

Lectures: 3 Hrs./Week

Credit: 3

Unit 1:
History of MicroElectroMechanical Systems (MEMS), market for MEMS, basics of microtechnology, lithography and etching techniques,

Unit 2:
principles of bulk and surface micromachining: subtractive processes, additive processes (evaporation, sputtering, epitaxial growth). Fundamental devices and processes, Multi User MEMS Process (MUMPs), SUMMiT: design rules; applications; micro hinges and deployment actuators,

Unit 3:
CMOS MEMS, cleanroom lab techniques, MicroOptoElectroMechanical Systems (MOEMS), bioMEMS and biomaterials, piezoresistivity; scanning probe microscopy, scaling laws, applications.

Unit 4:
Lumped element modeling and design, Electrostatic Actuators , Electromagnetic Actuators, Linear and nonlinear system dynamics, resonant systems, Elasticity (stress, strain, material properties), Mechanical structure basics (bending of beams, torsion, natural frequency), Optical system design basics (Gaussian beam optics, matrix optics, resolution)

Unit 5:
Application case studies: MEMS Scanners and Retinal Scanning Displays (RSD), Grating Light Valve (GLV), Digital Micromirror Devices (DMD),

Unit 6:
Optical switching, Capacitive Micromachined Ultrasonic Transducers (CMUT)

Reference Books:

M.Tech Electronics Technology Syllabus w.e.f from Academic year 2012-2013
Semester II

E 24 (E) Robotics and Machine Vision

Teaching Scheme
Examination Scheme
Lectures: 3 Hrs./Week
Credit: 3

UNIT 1

UNIT 2
Kinematics of Robot: Introduction, Matrix Representation, Homogeneous transformation, forward and inverse Kinematics, Inverse Kinematics Programming, Degeneracy, dexterity, velocity and static forces, velocity transformation force control systems, Basics of Trajectory planning.

UNIT 3

UNIT 4

UNIT 5
Image processing Techniques: Data reduction – Windowing, digital conversion.
Segmentation – Thresholding, Connectivity, Noise Reduction, Edge detection, Segmentation, Region growing and Region Splitting, Binary Morphology and grey morphology operations.

UNIT 6
Feature Extraction: Geometry of curves – Curve approximation, Texture and texture analysis,
TEXT BOOK


REFERENCES

Semester II

Elective –II

E25(V) RF Integrated Circuit Design

Teaching Scheme
Lectures: 3 Hrs./Week
Credit: 3

Unit 1:
Introduction to MOSFET Devices, MOSFET modeling, Spice model, Device parasitics, RF modeling, Parasitics sensitive to RF.

Unit 2:
Issue in RF IC a brief review, Impedance matching, use and design of passive circuits, LNA Design.

Unit 3:
Matching Techniques using algebra techniques, Basic Bond circuits, UHF Mixer design.

Unit 4:
Cross talk, Cross connect architecture, Cross Connect characteristics, classification, Cross connect mechanism, Cross connect mitigation, Cross connect reduction, multiple Cross connect sources.

Unit 5:
EMI, EMC, Importance in ASIC Design, Introduction, EDA Tool in ASIC Design,

Unit 6:
Design Flow, testing, Environment, sources of EMI/RFI, Solutions.

References
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M.TECH (Electronics Technology) PROGRAMMES

Semester II

E 25 (V) VLSI in Signal Processing

Teaching Scheme Examination Scheme
Lectures: 3 Hrs./Week Credit: 3

Unit 1:
Typical DSP algorithms and representation : DCT, DWT and filter banks, Vector Quantization, Block diagram, signal flow graph, data flow graph and dependence graph.

Unit 2:
DSP application demands and CMOS technologies, Loop bound and iteration bound and their computation, Pipelining and Parallel Processing: Pipelining of FIR Digital filters, parallel FIR digital filters, combined pipelining and parallel processing.

Unit 3:
Retiming, Properties of retiming, Retiming techniques for clock minimization and register minimization. Unfolding, properties and applications of unfolding.

Unit 4:
Folding, 2D Systolic arrays and matrix multiplication, Bit level arithmetic architectures: Parallel multipliers, Baugh Wooley carry save multiplier, Booth Wallace Tree multipliers, Bit serial multipliers, Bit serial FIR filter. Carry free radix-2 addition and subtraction,

Unit 5:
Floating point arithmetic, Clocking for synchronous pipelining and wave pipelining systems, Clock distribution, Floor planning.

Unit 6:
FPGA architectures: block memories, CLBs, IOBs, Routing resources, specific resources like MAC, DLL, clock managers etc.

References books:


M.Tech Electronics Technology Syllabus w.e.f from Academic year 2012-2013
Semester II
E 25 (E) High Performance Networks

Teaching Scheme
Examination Scheme

Lectures: 3 Hrs./Week
Credit: 3

Unit 1:
Types of Networks, Network design issues, Data in support of network design. Network design tools, protocols and architecture.

Unit 2:

Unit 3:
Introduction, challenges, SCSI protocols and architecture: RAID, Backup and mirroring, Fiber channel attached storage. Network attached storage including NFS, CIFS and DAFS, Management of network storage architectures. New storage protocols, architectures and enabling technologies.

Unit 4:
Introduction to CDMA and spread spectrum system, CDMA standards, system architectures of wireless communication systems, physical, network and data link layer of CDMA, wireless LAN standards: IEEE 802.11b, ARPA.

Unit 5:

Unit 6:
A model for internet security, security attacks, services, internet standards & RFCs, Cryptography, Conventional encryption, principles and algorithms, cipherblock, modes of operation, location of encryption devices, key distribution, Public key cryptography principles and algorithms, RSA algorithm.

Reference Books:

M.Tech Electronics Technology Syllabus w.e.f from Academic year 2012-2013
Semester II
E 25 (E) Mobile Computing

Teaching Scheme
Examination Scheme
Lectures: 3 Hrs./Week
Credit: 3

Unit 1:
1G to 4G mobile telephone technologies.

Unit 2:
Reference architectures for wireless LAN, WLANTPRS.

Unit 3:
GSM and VOIP architecture, 4-G LTE network architecture and protocols

Unit 4:
Transmit diversity and MIMO spatial multiplexing,

Unit 5:
Applications of Mobile computing Business value behind mobile application development Best practices for the entire project life cycle.

Unit 6:
Casestudies secure mobile application development Fundamentals of wireless Mark up language WML script applications.

Reference Books:
1. Introduction to Mobile Telephone Systems, 2nd Edition, 1G, 2G, 2.5G, and 3G Technologies and Services by Lawrence Harte
2. Wireless and Mobile Data Networks by Aftab Ahmad
3. Wireless and Mobile Network Architectures by Yi-Bing Lin and ImrichChlamtac
5. Mobile IP Technology and Applications by Stefan Raab and Madhavi W. Chandra
   1. WML &WMLScript: A Beginner's Guide by Kris A. Jamsa

M.Tech Electronics Technology Syllabus w.e.f from Academic year 2012-2013
Semester I & II
S 16 & S 26 Seminars

Teaching Scheme
Contact hrs : 2 Hrs./Week/student
Credit: 2

Students shall deliver Seminar on the State-of-the-Art topic in front of Examiners and Student-colleagues. Prior to presentation, he/she shall carry out the detailed literature survey from Standard References such as International Journals and Periodicals, recently published reference Books etc. and submit a report on the same along with computer based presentation copy to the concerned examiner/guide at the end of the seminar. The assessment shall be based on selection of topic, its relevance to the present context, report documentation and presentation skills.

Guide should spare (Guide) for 2hrs/week/student for seminar.
T 31 Industrial Training:

Teaching Scheme
Examination Scheme
Contact hrs : 2 Hrs./Week/student
Credit: 4

8 Weeks at the end of First Year and as a part of evaluation at the end of third semester student should submit the report for the 8 week industrial training and give presentation to the concern guide, concern guide should spare 2hrs/week/student
The student shall be allowed to submit the dissertation phase I report only after the completion of minimum 50% work of the total project with intermediate /partial results of the dissertation project to the concern guide and the dissertation phase II report only after the full-fledge demonstration of his /her work to the concerned guide. Assessment of the dissertation shall be based on design & implementation aspects, documentation & presentation skills, utility of the dissertation work & publications based on the same.
For the dissertation phase I and phase II concern guide should guide to each student minimum for 2 hrs per week till the final submission of the dissertation of the concern student.
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</tbody>
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</tr>
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