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दुरध्वी: (ईपीएबीएक्स) २६०९००० (अभ्यास मंडळे विभाग- २६०९०९४) तार : युनिशिवाजी
फॅक्स : ००९१-०२३१-२६९१५३३ व २६९२३३३.e-mail:bos@unishivaji.ac.in

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(2009)

Ref.No./SU/BOS/ENGG/4480 Date :08-08-2013

The Principal,
Aannasaheb Dange
College of Engineering & Technology,
At/Po. Ashta, Tal-Walwa,
Dist - Sangli.

Sub : Regarding Structure and Syllabus of M.E. (VLSI and Embedded Systems) Sem I to IV under the Faculty of Engineering & Technology.

Sir,

With reference to the subject mentioned hereabove , I am directed to inform you that the University authorities have accepted & granted approval to the Structure and Syllabus of M.E. (VLSI and Embedded Systems) Sem I to IV (to be implemented from the academic year 2013-14) under the Faculty of Engineering & Technology.

It is also hereby informed that the above Structure & Syllabus is available on the University website **http://www.unishivaji.ac.in i.e. ONLINE SYLLABUS link.**

You are therefore requested to bring this to the notice of all the teachers and students concerned.

Thanking you,

Yours faithfully,
Sd/-
Dy. Registrar

Encl: As above
Copy to:
1. Dean, Faculty of Engineering & Technology } For information
2. Chairman, BOS in Electronics Engineering.
3. Appointment Section
4. O. E. 4 Section } For information and necessary action.
5. Affiliation Section
6. Eligibility Section

Shivaji University Kolhapur

Syllabus for

M.E. in

VLSI and Embedded Systems

Introduced from June 2013

M.E. (VLSI AND EMBEDDED SYSTEMS) STRUCTURE

Teaching and Evaluation Scheme

SEMESTER – I

SR.NO	SUBJECT	TEACHING SCHEME					EXAMINATION SCHEME				
		L	T	P	Total	Credits	Paper	TW	POE	OE	Total
•	CMOS VLSI Design-I	3	-	2	05	**04**	100	25	-	25	150
•	Advanced Digital Signal Processing	3	-	2	05	**04**	100	25	50	-	175
•	Advanced Embedded Systems	3	-	2	05	**04**	100	25	50	-	175
•	Digital System Engineering	3	1	-	04	**04**	100	25	-	-	125
•	Elective-1	3	1	-	04	**04**	100	25	-	-	125
•	Seminar-I	-	-	02	02	**02**	-	50	-	-	50
	TOTAL	**15**	**02**	**08**	**25**	**22**	**500**	**175**	**100**	**25**	**800**

SEMESTER - II

SR. NO	SUBJECT	TEACHING SCHEME					EXAMINATION SCHEME				
		L	T	P	Total	Credits	Paper	TW	POE	OE	Total
•	CMOS VLSI Design-II	3	-	2	05	**04**	100	25	50	-	175
•	Analog & Mixed Signal Design	3	-	2	05	**04**	100	25	50	-	175
•	Embedded Software Design	3	-	2	05	**04**	100	25	-	25	175
•	Testing & Testability	3	1	-	04	**04**	100	25	-	-	125
•	Elective-II	3	1	-	04	**04**	100	25	-	-	125
•	Seminar-II	-	-	2	02	**02**	-	50	-	-	50
	TOTAL	**15**	**02**	**08**	**25**	**22**	**500**	**175**	**100**	**25**	**800**

Note: Seminar-II should be based on Industrial training (of minimum 2 weeks) / dissertation related topic (in consultation with guide) / departmental project.

SR. NO.	SUBJECT	TEACHING SCHEME					EXAMINATION SCHEME				
		L	T	PR	Total	Credits	Paper	TW	POE	OE	Total
1.	Phase I Seminar (Synopsis Submission)	-	-	2	02		-	50	-	-	50
2.	Progress Seminar I & demonstration	-	-	3	03		-	100	-	-	100
	TOTAL	**-**	**-**	**05**	**05**		**-**	**150**	**-**	**-**	**150**

SEMESTER - III

SR. NO.	SUBJECT	TEACHING SCHEME					EXAMINATION SCHEME				
		L	T	PR	Total	Credits	Paper	TW	POE	OE	Total
1.	Progress seminar II & demonstration	-	-	05	05		-	50	-	-	50
2.	Pre-submission presentation & demonstration	-	-	-	-		-	100	-	-	100
3.	Final Viva-Voce	-	-	-	-		-	-	200	-	200
	TOTAL	**-**	**-**	**05**	**05**		**-**	**150**	**200**	**-**	**350**

SEMESTER - IV

Note:

- T.W. marks shall be based on the work carried out by the candidate based on his/her dissertation work in consultation with his/her guide. This work may also include related software assignment, hardware implementation, field work, industrial training etc. as decided by the guide. The student shall submit the progress report to the department. The student shall deliver a seminar at least twice in a semester and demonstrate the partial accomplishment of the dissertation work.
- Except for final Viva-voce which is conducted by external examiner and Internal Examiner appointed by SUK, all other evaluations will be done by the concerned departmental team as TW assessment.

List of Elective Subjects for Semester I and II

Sr. No.	Elective-I	Elective-II
1	DSP VLSI-I	DSP VLSI-II
2	System on Chip Architecture-I	Automotive Embedded Systems
3	Communication System Design	Low power VLSI design
4	Algorithms for VLSI Design Automation	System on Chip Architecture-II

Note: Students opting for DSP VLSI-II/ SoCA-II in the second semester must opt for DSP VLSI-I/ SoCA-I in the first semester as elective, else other options are open.

M.E. (VLSI and Embedded Systems) Semester-I

CMOS VLSI Design-I

Lectures: 3 Hrs/week
Practical: 2 Hrs/week

Theory: 100 marks
Term Work: 25 marks.

OE: 25 Marks

Unit	Contents	Hrs
1	**MOS Transistor Theory:** Physical structure of MOS transistor, MOS transistor under static conditions, secondary effects, SPICE models for MOS transistor, Process variation, Technology Scaling	4
2	**CMOS Inverter:** CMOS inverter, Static and Dynamic behavior of CMOS inverter, Power, Energy and Energy-Delay, Technology Scaling and Impact on inverter Metrics	6
3	**CombInational Logic Designs in CMOS:** Static CMOS design, Dynamic CMOS Design, Examples	6
4	**Sequential Logic Designs in CMOS:** Introduction, Static latches and registers, Dynamic latches and registers, Pipelining, non-bistable sequential circuits, Examples	8
5	**Designing Arithmetic Building Blocks:** Adders, Multipliers, Shifters, Power and Speed Trade-Off in Datapath Structures	8
6	**The Manufacturing Process:** Manufacturing CMOS integrated circuits, design rules, packaging integrated circuits, trends in process technology	6

Text book:

"Digital integrated circuits- A design perspective", Jan Rabaey, Anantha C, 2nd edition, PHI

Reference books:

- "Essentials of VLSI Circuits and Systems", Kamran Eshraghian, Pucknell and Eshraghian, Prentice-Hall (India)
- "CMOS Digital Integrated Circuits: Analysis and Design", Kang, Leblebici, TATA McGRAW Hill.
- "Modern VLSI Design", Wayne Wolf, Pearson Education
- "CMOS VLSI Design", Neil Wieste, David Harris, Ayan Banerjee, Pearson Education, 3rd Edition, 2008

List of experiments (Using FPGA Tools)	Sessions
• Design of Combinational Circuits • Adder (Carry look-ahead adder) ii) Substractor iii) Multiplexer	**6 sessions (Self Study)**
• Design of Sequential Circuits • 16-bit universal shift register ii) 16-bit binary Counter/Gray counter	

- Design of 8-bit ALU
  Arithmetic functions (Adder, Incrementer, Subtractor, Decrementer)
  Multiplier (Robertson's/Booth's algorithm)
  Logical functions (Inverter, AND,OR,XOR, NAND, NOR, XNOR)
- Design of Control Unit
  - Behavior description ii) Sequential Design using FSM method

4 Sessions (Self Study)

- Design of Memory units
  - ROM (512 x 8) ii) SRAM (1024 x 8)

- Building all components to design 8-bit processor with following instructions
  - MOVE R1 to R2 ii) MOVE immediate data
  - LOAD ACCMULATOR iv) MOVE memory to ACC
  - MOVE AC to Memory vi) Add
  - Subtract viii) Multiply
  - Logical AND, OR, NAND, NOR, XOR, XNOR, invert
  - Decrement xi) Increment
  - Jump to addr xiii) NOP
  - Halt

Miniproject

- Demonstration of ASIC tools(Microwind and Mentor Graphics Tools)

2 sessions

- Layout Design, Simulation , RC extraction using ASIC tools for
  - Inverter Equal area, Equal Speed
  - 2-input NAND , 2-input XOR
  - 2.input AND using pass transistor and transmission gate Comparison
  - 2-input XOR using T-gate
  - Full Adder
  - 4-bit comparator
  - D-latch, D-register
  - 3-bit counter
  - Schmitt Trigger, Astable Circuit, Monostable Circuit

10 sessions

Reference Books for experiments:

- "VHDL", Douglas Perry, 4th Edition, McGraw Hill Publication
- "VHDL Primer", Jayram Bhaskar, McGraw Hill Publication, 3rd Edition, 2009, (e_book available on http://www.ziddu.com/download/15978324/AVHDLPrimerbyJ.Bhaskar)
- "Xilinx on line Manuals".(www.Xilinx.com)
- "Xilinx Download Kit (Spartan 3-E) Manual" ".(www.Xilinx.com)
- Manuals for Magic, Tanner tool, Mentor Graphics etc for corresponding websites

M.E. (VLSI and Embedded Systems) Semester-I

Advanced Digital Signal Processing

Lectures: 3 Hrs/week
Practical: 2 Hrs/week

Theory: 100 marks
Term Work: 25 marks.
POE: 50 Marks

Unit	Contents	Hrs
1	**The Discrete and Fast Fourier Transform:** Frequency domain sampling and reconstruction of discrete time signals, discrete Fourier transform, DFT as linear transform, relationship of DFT with other transforms, properties of DFT, linear filtering methods based on DFT , frequency analysis using DFT, FFT algorithms: radix 2 radix 4,split radix FFT, applications of FFT algorithms, a linear filtering approach to computation of DFT: Goertzel Algorithm, chirp z transform algorithm.	8
2	**Design of Digital Filters:** General considerations: causality and its implication, characteristics of practical frequency selective filters, Design of FIR filters: Linear phase FIR filters using windowing, frequency sampling, optimum equiripple FIR filter, FIR differentiator, Hilbert Transform, Design of digital filters based on Least square methods: pade approximation, Least square design methods, FIR least square inverse filters, Design of IIR filters in frequency domain.	8
3	**Adaptive Systems:** Adaptive systems-Definition and characteristics, areas of applications, general properties, open and closed loop adaptation, applications of closed loop adaptation. The adaptive liner combiner-General description, input signal and weight vectors, desired response and error, the performance function, gradient and minimum mean square error. Example of performance surface, alternative expression of the gradient, de-correlation of error and input components.	8
4	**Theory of Adaptation and Adaptive Algorithms:** Properties of the quadratic performance surface-Normal form of the input correlation matrix, eigen values and eigen vectors of the input correlation matrix, an example with two weights, Searching the performance surface-Methods of searching the performance surface, basic ideas of gradient search methods, a simple gradient search algorithm and its solution, stability and rate of convergence, Wiener filters: Linear Optimum Filtering, Statement of the problem, Principle of Orthogonality, Minimum Mean-Square Error Adaptive algorithms and structures: The LMS algorithms, RLS algorithm	8
5	**Multirate Signal Processing:** Introduction, decimation by factor D, interpolation by factor I, sampling rate conversion, filter design and implementation for sampling rate, applications of multirate filters.	5
6	**Power Spectrum Estimation:** Estimation of spectra from finite duration observation of signal. Computation of energy density function, Estimation of autocorrelation and power spectrum of random signals, the period gram. Use of DFT in power spectrum estimation. Parametric method of power spectrum estimation. • Unconstrained least square methods for AR model parameters. • MA model for power spectrum estimation. • ARMA model for power spectrum estimation	8

Reference Books:

- "Advanced Digital Signal Processing", Proakis, Prentice Hall International.
- "Discrete Time Signal Processing", Oppenheim Schafer, Pearson Education.
- "Adaptive Filter Theory"- S. Haykin, Pearson Education, 4th Edition
- "Adaptive Signal Processing", - B. Windrow, S.D. Sterns, Pearson Education.
- "Digital Signal Processing", Sanjit K. Mitra Tata McGraw-Hill Publication.

***Minimum 10 experiments can be conducted based on the syllabus wherein 2 experiments should be on DSP processors.**

M.E. (VLSI and Embedded Systems) Semester-I

Advanced Embedded Systems

Lectures: 3 Hrs/week
Practical: 2 Hrs/week

Theory: 100 marks
Term Work: 25 marks.
POE: 50 Marks

Unit	Contents	Hrs
1	**Introduction to Embedded Systems & ARM Processors** Embedded system (ES) definition, Embedded System Evaluation, ES Types with examples, Distinguish a Real Time Embedded System from other systems, Components of an Embedded system, Embedded system design issues & Design flow, a comparative study ARM7TDMI, ARM8, ARM9TDMI, ARM10TDMI, ARM11	4
2	**Bootloader, Firm- ware and OS** Firmware execution flow, ARM firmware suit, Redhat RedBoot, an introduction to operating systems, fundamental components of OS, case study of simple operating system.	6
3	**ARM Cache Memory Systems** Memory hierarchy, Cache Architecture, Cache policy, CP15 and Caches, Flushing and cleaning cache, Cache lock down, Cache Performance , Memory protection unit, Memory management unit, Virtual memory	8
4	**SOC Architecture LPC3250** Bus architecture and memory map, System control block, Clocking and power control, external memory controller, NAND flash controller, LCD controller	8
5	**MSP430** Architecture, Key features of the MSP430x1xx, Flexible Clock System, Embedded Emulation, Address Space, Flash, RAM, Peripheral Modules, Special Function Registers (SFRs), Memory Organization, System Reset and Initialization, Power-On Reset (POR), Brownout Reset (BOR), Device Initial Conditions After System Reset, Interrupts (Non)- Maskable Interrupts (NMI), Maskable Interrupts, Interrupt Processing, Interrupt Vectors.	8
6	**RISC 16-Bit CPU** CPU Introduction, CPU Registers, Program Counter (PC),Stack Pointer (SP),Status Register (SR), Constant Generator Registers CG1 and CG2 General−Purpose Registers R4 - R15, Addressing Modes Register Mode, Indexed Mode, Symbolic, Absolute Mode, Indirect Register, Indirect Auto-increment Mode, Immediate Instruction, Double-Operand (Format I) Instructions, Single-	10

Operand (Format II)Instructions, Jumps, Instruction Cycles and Instruction Set Description.

Reference Books:

- "ARM System Developers Guide- Designing & Optimizing System Software", Andrew N., Dominic Sloss, and Chris Wright, Elsevier, 2010.
- ARM9EJ-S Technical reference manual
- LPC32x0 User manual (www.nxp.com/documents/application_note/AN10902.pdf)
- MSP 430 User Guide (www.ti.com/lit/ug/slau278o/slau278o.pdf)

Note: The Experiments can be conducted based on the following guidelines.

Experiments	Minimum number of Experiments
• Assembly language programming	04
• C-programming	04
• MSP-430	04
• Protocol design	02

M.E. (VLSI and Embedded Systems) Semester-I

Digital System Engineering

Lectures: 3 Hrs/week
Tutorial: 1 Hr/ week

Theory: 100 marks
Term Work: 25 marks.

Unit	Contents	Hrs
1	**Wires** Geometry and Electrical properties, Electrical models of wires (Ideal wire, Transmission line), Simple transmission lines (RC, lossless LC, Lossy LRC transmission lines, Dielectric absorption), Special transmission lines (Multidrop buses, Balanced Transmission lines, Common and differential mode impedance, Isolated lines)	6
2	**Noise in Digital Systems** Noise sources in a digital system, Power Supply Noise, Cross-talk, Inter-symbol Interference, Noise due to other sources (Alpha particles, Electro-magnetic Interference, Process variation, Thermal Noise, Shot Noise, Flicker or 1/f Noise), Managing noise.	6
3	**Signaling Conventions** CMOS and Low swing current mode signaling system, Considerations in transmission system design, Signaling modes for transmission lines, Transmitter signaling methods, Receiver signal detection, Source termination, Under-terminated Drivers, Differential Signaling, Signaling over capacitive transmission medium, Signal encoding	8
4	**Timing Conventions** Conventional Synchronous system and closed loop pipelined system, Considerations in timing design, Timing fundamentals, Timing properties of combinational logic and clock storage elements, Eye diagram, Encoding Timing	8

(Signals and Events), Open loop synchronous timing, Closed loop timing, Phase locked loops, Clock Distribution

5	**Synchronization** Synchronization Fundamentals, Applications of synchronization (Arbitration of asynchronous signals, Sampling asynchronous signals, Crossing clock domains), Synchronization failure and meta-stability, Synchronizer Design (Mesochronous, Plesiochronous, Periodic Asynchronous)	**8**
6	**Power Distribution** The power supply network (Local loads, Signal loads), Local Regulation, Logic loads and on-chip power supply distribution.	**4**

Textbook:

"Digital System Engineering", William Dally and John Poulton, Cambridge University Press, Reprint 2007

References:

- "High Speed Digital Design"- A Handbook of Black Magic, Howard W. Johnson, Martin Graham, Prentice Hall PTR, Englewood Cliffs, NJ 0763
- "High Speed Digital System Design: Interconnect Theory and Design Practices" Stephen H. Hall, Garrett W. Hall, James A. McCall, Wiley-IEEE Press (ISBN: 978-0-471-36090-2

***At least 8 Tutorials should be conducted based on above syllabus**

M.E. (VLSI and Embedded Systems) Semester-I

DSP VLSI-I

Elective I

Lectures: 3 Hrs/week **Theory:** 100 marks
Tutorial: 1 Hr/ week **Term Work:** 25 marks.

Unit	Contents	Hrs
1	**DFG representation and Iteration Bound** DFG, loop bound and iteration bound, Algorithm for computing iteration bound, (Longest path algorithm, Minimum cycle algorithm), Iteration bound for multirate DFGs	**4**
2	**Pipelining and Parallel Processing** Pipelining for FIR digital filters, Data broadcast structures, Fine grain pipelining, Parallel processing, Pipelining and parallel processing for low power, Combining pipelining and parallel processing	**6**
3	**Retiming** Definitions and properties, Solving system of inequalities, Retiming techniques , cutset retiming and pipelining, Retiming for clock period minimization, Retiming for register minimization	**8**
4	**Unfolding** Concept behind unfolding, an algorithm for unfolding, Properties for unfolding, Applications for unfolding, Sample period reduction, Word level parallel processing, bit-level parallel processing	**8**

5	**Folding** Introduction to folding, Folding Transformation, Lifetime Analysis for Register minimization in folded architecture, Folding of multi-rate DSP systems	**8**
6	**Systolic Array Design** Systolic Array Design Methodologies, Family of systolic arrays (FIR filter) using linear mapping techniques, Matrix – Matrix Multiplication	**4**

Text Book:

"VLSI Digital Signal Processing- Design and Implementation" , Keshav K. Parhi, Wiely (India) 2007

Reference Book:

"VLSI Synthesis of DSP kernels- Algorithms and Architectural Transformations", Mahesh Mehendale, Sunil Sherlekar, Kluwer Publications, 2002

***At least 8 Tutorials should be conducted based on above syllabus**

M.E. (VLSI and Embedded Systems) Semester-I

System on Chip Architecture-I

Elective I

Lectures: 3 Hrs/week **Theory:** 100 marks
Tutorial: 1Hr/week **Term Work:** 25 marks

Unit	Contents	Hrs
1	**Introduction & Bus based Communication Architectures** Trends in System-On-Chip Design, Coping with Soc Design Complexity, ESL Design Flow, On-Chip Communication Architectures: A Quick Look, Characteristics of Bus-Based Communication Architectures, Data Transfer Modes, Bus Topology Types, Physical Implementation of Bus Wires, Buses in the DSM Era.	**6**
2	**On-Chip Communication Architecture Standards** Standard On-Chip Bus-Based Communication Architectures, Socket-Based On-Chip Bus Interface Standards, Discussion: Off-Chip Bus Architecture Standards	**6**
3	**Models for Performance Exploration** Static Performance Estimation Models, Dynamic (Simulation-Based) Performance Estimation Models, Hybrid Communication Architecture Performance Estimation Approaches	**8**
4	**Models for Power and Thermal Estimation** Bus Wire Power Models, Comprehensive Bus Architecture Power Models, Bus Wire Thermal Models, PVT Variation-Aware Power Estimation	**6**
5	**Synthesis of On-Chip Communication Architectures** Bus Topology Synthesis, Bus Protocol Parameter Synthesis, Bus Topology and Protocol Parameter Synthesis, Physical Implementation Aware Synthesis, Memory–Communication Architecture Co-synthesis, Physical and Circuit Level Design of On-Chip Communication Architectures	**8**
6	**Encoding Techniques for On-Chip Communication Architectures** Techniques for Power Reduction, Techniques for Reducing Capacitive Crosstalk Delay, Techniques for Reducing Power and Capacitive Crosstalk Effects,	**6**

Techniques for Reducing Inductive Crosstalk Effects, Techniques for Fault Tolerance and Reliability

Text Book:

"On-Chip Communication Architectures: System on Chip Interconnect", Sudeep Pasricha and Nikil Dutt, Morgan Kaufmann Publishers © 2008

Reference Books:

- "Transaction Level Modeling with SystemC: TLM Concepts and Applications for Embedded Systems", Frank Ghenassia, Springer © 2005 (281 pages), ISBN:9780387262321
- "Networks on Chips: Technology and Tools", Luca Benini and Giovanni De Micheli, Morgan Kaufmann Publishers © 2006 (408 pages), ISBN:9780123705211,

***Minimum 8 tutorials can be conducted based on the above syllabus**

M.E. (VLSI and Embedded Systems) Semester-I

Communication System Design

Elective I

Lectures: 3 Hrs/week **Theory:** 100 marks
Tutorial: 1 Hr/week **Term Work:** 25 marks

Unit	Contents	Hrs
1	**Introduction** Circuit designers perspective of communication system: Wireless channel description, path loss, multi path fading	4
2	**Receivers** Receiver front End in general, Filter Design, Non idealities and Design Parameters of receiver front end, Derivation of NF, IIP_3 of Receiver Front End, Partitioning of required NF_{rec_front} and IIP_{3,rec_front} into individual NF & IIP_3	6
3	**Low Noise Amplifier** Introduction, Wideband LNA Design, Narrow band LNA: Impedance Matching, Narrowband LNA: Core Amplifier	6
4	**Active Mixers** Introduction, Balancing, Qualitative Description of Gilbert Mixer, Conversion Gain, Distortion-Low Frequency Case: Analysis of Gilbert Mixer, Distortion-High Frequency Case, Noise, A Complete Active Mixer	6
5	**Analog to Digital Converters** Demodulators, A to D Converters used in receivers, Low cost Sigma delta modulators and its implementation.	6
6	**Frequency Synthesizers & Loop Filters** Introduction to VCO, LC oscillators, ring oscillator, phase noise, general description of loop filter, its design approaches, a complete synthesizer design example.	8

Text Book:

"VLSI for Wireless Communication" Bosco Leuing, Pearson Education

Reference Books:

- "Design of CMOS Radio Frequency Integrated Circuits", T Lee, Cambridge Univ.Press
- "Analysis and Design of Analog Integrated Circuits", P Gray and R Meyer, John Wiley & Sons
- "Microelectronics Transistor Amplifier", Analysis and design G Gonzalez, Prentice Hall

***At least 8 Tutorials should be conducted based on above syllabus**

M.E. (VLSI and Embedded Systems) Semester-I

Algorithms for VLSI Design Automation

Elective I

Lectures: 3 Hrs/week **Theory:** 100 marks
Tutorial: 1 Hr/week **Term Work:** 25 marks.

Unit	Contents	Hrs
1	**Logic Synthesis & Basic Algorithms** Introduction to combinational logic synthesis, Binary Decision Diagram, Hardware models for High-level synthesis, graph algorithms, computational geometry algorithms.	6
2	**Partitioning** Problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms	6
3	**Placement, Floor Planning & Pin Assignment** Problem formulation, simulation base placement algorithms, other placement algorithms, constraint based floor planning, floor planning algorithms for mixed block & cell design. General & channel pin assignment for register minimization	8
4	**Global Routing** Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches	6
5	**Detailed Routing** Problem formulation, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms	6
6	**Over The Cell Routing & Via Minimization and Compaction** Two layers over the cell routers, constrained & unconstrained via minimization, problem formulation, one-dimensional compaction, two dimension based compaction, hierarchical compaction	8

Text Book:

"Algorithms for VLSI physical design Automation", Naveed Shervani, Kluwer Academic Publisher, Second edition.

Reference Books:

- "Algorithm and Data Structures for VLSI Design", Christophn Meinel & Thorsten Theobold, Kluwer Academic publisher, 2002
- "Evolutionary Algorithm for VLSI", Rolf Drechsheler Kluwer Academic publisher, Second edition
- "Introduction to CAD for VLSI", Trimburger, Kluwer Academic publisher, 2002
- "VLSI Design & EDA tools", Angsuman Sarkar, Swapnadeep De, Scitech Pubisher.

***At least 8 Tutorials should be conducted based on above syllabus**

M.E. (VLSI and Embedded Systems) Semester-II

CMOS VLSI Design-II

Lectures: 3 Hrs/week
Practical: 2 Hrs/week

Theory: 100 marks
Term Work: 25 marks.
POE: 50 Marks

Unit	Contents	Hrs
1	**The wire** Introduction, interconnect parameters-capacitance, resistance, inductance, electrical wire models, spice wire models	6
2	**Coping with Interconnects** Capacitive Parasitics, Resistive Paracitics, Inductive Paracitics, Advanced interconnect techniques	6
3	**Designing Memory and Array Structures** Introduction, the Memory Core, Memory Peripheral Circuitry, Memory Reliability and Yield, Power Dissipation in Memories.	6
4	**Timing issues in Digital Circuits** Timing classification of digital systems, synchronous design, self timed circuit design	6
5	**Synchronizers & Arbiters** Concept and implementation, clock synthesis & synchronization using PLL, future directions & perspectives	8
6	**Implementation Strategies for Digital ICs** From custom to semicustom & structured array design approaches, custom circuit design, cell based design methodology, array based implementation approaches	8

Text Book:

"Digital integrated circuits- A design perspective", Jan Rabaey, Anantha, 2nd edition, PHI

Reference Books:

- "Essentials of VLSI Circuits and Systems", Kamran Eshraghian, Pucknell and Eshraghian, Prentice-Hall (India)
- "CMOS Digital Integrated Circuits: Analysis and Design", Kang, Leblebici, TATA McGRAW Hill.

- "Modern VLSI Design", Wayne Wolf, Pearson Education
- "CMOS VLSI Design", Neil Weste, David Harris, Ayan Banerjee, Pearson Education, 3rd Edition, 2008

Experiments:

- Physical level design of various 16-bit adder architectures (any 5)
    - Carry propagate adder
    - Carry propagate adder using inversion property
    - Carry bypass adder
    - Carry select adder
    - Manchester carry chain adder
    - Carry look ahead adder
- Multiplier architecture
    - Wallace tree
    - Array multiplier
    - Bit serial architecture
    - Distributed arithmetic approach
- Memory design
    - SRAM-64 bytes- extend it to 1Kbytes
    - DRAM- 64 bytes- extend it to 1Kbytes
    - Comparison of above two
- Design & implement self timed circuit & compare timing parameters of same circuit

M.E. (VLSI and Embedded Systems) Semester-II

Analog and Mixed Signal Design

Lectures: 3 Hrs/week
Practical: 2 Hrs/week

Theory: 100 marks
Term Work: 25 marks.
POE: 50 Marks

Unit	Contents	Hrs
1	**Single Stage Amplifier** CS stage with resistance load, divide connected load, current source load, triode load, CS stage with source degeneration, source follower, common-gate stage, cascade stage, choice of device models.	6
2	**Differential Amplifiers** Basic difference pair, common mode response, Differential pair with MOS loads, Gilbert cell.	4
3	**Passive and Active Current mirrors** Basic current mirrors, Cascade mirrors, active current mirrors.	4
4	**Frequency Response of CS Stage** Source follower, Common gate stage, Cascade stage and Difference pair. Noise in CS stage, C- G stage, source follower, cascade stage, differential pair.	6
5	**Operational Amplifiers** One Stage OP-Amp. Two Stage OP-Amp, Gain boosting, Common Mode Feedback, Slew rate, PSRR. Compensation of 2stage OP-Amp, Other compensation techniques.	6
6	**Oscillators** Ring Oscillators, LC Oscillators, VCO, Mathematical Model of VCO.	4

Reference Books:

1. “Design of Analog CMOS Integrated Circuits”, Behzad Razavi, TMH, 2007.
2. “CMOS Circuit Design, Layout, and Simulation”, R. Jacob Baker, Wiley Publication, 2010
3. NPTEL video lectures of IITM on Analog and Mixed Signal Design

Experiments:

Note: All experiments should be implemented on one of the ASIC tools like- CADANCE/ SYNOPSIS/ MENTA GRAPHICS/Microwind, Tanner etc.

- Design the MOS transistor circuits for DC & AC small signal parameters, completing the design flow mentioned below:
    - Draw the schematic and verify the following
        - DC Analysis
        - AC Analysis
        - Transient Analysis
    - Draw the Layout and verify the DRC, ERC
    - Check for LVS
- Design a **TWO** stage **op-amp** with given specification using given differential amplifier Common source and Common Drain amplifier in library and completing the design flow mentioned below:
    - Draw the schematic and verify the following
      i) DC Analysis
      ii). AC Analysis
      iii) Transient Analysis
    b. Draw the Layout and verify the DRC, ERC
    c. Check for frequency response, slew rate, offset effects and Noise.
3. Design a simple sample and hold circuit and measure the switching times.
4. Design a PLL and measure all the parameters.
5. Design a simple ADC/DAC and measure the data conversion time.
6. Design 3-8 decoder using MOS technology.
7. Two experiments on PSoCs

***Any experiments can be added to supplement the theory. Above are the only guide lines.**

M.E. (VLSI and Embedded Systems) Semester-II

Embedded Software Design

Lectures: 3 Hrs/week
Practical: 2 Hrs/week

Theory: 100 marks
Term Work: 25 marks.
OE: 25 Marks

Unit	Contents	Hrs
1	**Introduction** Embedded system overview, Real time, Multitasking, Real time Kernel, design challenges, Processor Technology, Application Ares of embedded system, specialties of embedded system, Recent trends in embedded systems	6
2	**General Purpose Processor Software** Introduction, basic Architecture, Data path, control unit, memory, instruction execution, pipelining, super-scale and VLIW architecture, programmers view,- instruction set, program and data memory space, registers, I/O, interrupts, operating system, Development environment, design flow and tools, testing and debugging, Application specific instruction set processor(ASIPS), selecting microprocessor, general purpose processor design	8
3	**Overview of Embedded /Real time Operating Systems** Off-the shelf operating systems, commonalities of operating systems, portable operating system interface, difference in operating systems, Embedded operating systems, Embedded NT, windows Xp embedded, Embedded Linux, Real time	6

operating systems, QNX Neutrino, Vx works, MicroC/OS-II, RT Linux, Handheld operating systems, Palm OS, Symbian OS, windows CE.

4	**Software Architecture** Round Robin, Round Robin with interrupts, Function queue scheduling Architecture, Real time operating system architecture, selecting architecture, task and task states, task and data, semaphores, shared data and reentrancy, shared data problems.	**6**
5	**Operating System Services** Message Queues, Mailboxes, Saving power, Saving Memory space, scheduling, threads states, pending threads, context switching, Round Robin scheduling, priority scheduling, priority inversion, the priority inheritance protocol, priority ceiling protocol, assigning priorities, Dead line, Line driven scheduling, Rate monotonic scheduling, dead lock, watch dog timers.	**8**
6	**µCOS** Kernel Structure: Tasks, Task States, Task Level Context Switching, Locking and unlocking of scheduler, Idle Task, Statistics Task, Interrupts, Clock Tick, Initialization, Starting the OS. Task Management: Creating/ Deleting and Suspending/ Resuming Tasks, Task Stacks and checking, Changing Task's Priority, Time Management: Delaying/Resuming Task, System Time, Event Control Blocks: Initialization of ECB, Placing/Removing Task from ECB waitlist, Finding Highest Priority Task, List of Free ECB, Task State Management. Communication in **µ**COS-II	**8**

Reference Books:

- "Embedded System Design- A Unified Hardware & Software Introduction", Frank Vahid, John Wiley, 2002.
- "An Embedded Software Primer", David E. Simon, Pearson Education
- "Embedded/ Real-Time Systems: Concepts, Design & Programming", Dr. k V K K Prasad, Dreamtech Press
- "MicroC/OS-II The Real Time Kernel", Jim Labrosse, 2nd Edition, , CMP Books,
- "Fundamentals of Embedded Software", Daniel W. Lewis, Prentice Hall of India

***Minimum 10 experiments should be conducted based on the above syllabus.**

M.E. (VLSI and Embedded Systems) Semester-II

Testing and Testability

Lectures: 3 Hrs/week **Theory:** 100 marks
Tutorial: 1 Hr/week **Term Work**: 25 marks

Unit	Contents	Hrs
1	**Fault Modeling** Single stuck-at fault, test methods-simulation for design verification & test evaluation, modeling circuits for simulation, algorithms for fault simulation, statistical methods for fault simulation	6
2	**Combinational Circuit Test Generation** Algorithms and representation, redundancy identification, significant combinational ATPG algorithms, test generation systems, test compaction.	6
3	**Sequential Circuit Test Generation** ATPG for single clock synchronous circuits, time frame expansion method, simulation based sequential circuit ATPG	6
4	**DSP based Analog and Mixed Signal Testing** Functional DSP based testing, static ADC and DAC testing methods, realizing emulated instruments using Fourier transforms, CODEC testing, dynamic flash ADC testing FFT techniques.	8
5	**Memory Testing** Faults, memory test levels, fault modeling , memory testing	4
6	**Design for Testability** Scan design- rules, test for scan circuits, partial scan design, random logic BIST-process, BIST- pattern generation, built in logic block observers, memory BIST March test SRAM BIST, system configuration with boundary scan	8

Text book:

"Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", M. Bushnell and V. D. Agrawal, Kluwer Academic Publishers, 2000.

Reference books:

- "Digital Systems Testing and Testable Design", M. Abramovici, M. A. Breuer and A. D. Friedman, IEEE Press, 1990.
- "Introduction to Formal Hardware Verification", T. Kropf, Springer Verlag, 2000.
- "System-on-a-Chip Verification-Methodology and Techniques", P. Rashinkar, Paterson and L. Singh, Kluwer Academic Publishers, 2001.

***At least 8 Tutorials should be conducted based on above syllabus**

M.E. (VLSI and Embedded Systems) Semester-II

DSP VLSI- II

Elective II

Lectures: 3 Hrs/week **Theory:** 100 marks
Tutorial: 1 Hr/week **Term Work:** 25 marks

Unit	Contents	Hrs
1	**Fast Convolution** Introduction, Cook-Toom Algorithm, Winograd Algorithm, Iterated Convolution, Cyclic Convolution, Design of Fast Convolution Algorithm by Inspection.	4
2	**Algorithmic & Numerical Strength Reduction** Parallel FIR Filters, Discrete Cosine Transform and Inverse DCT. Parallel Architectures for Rank- Order Filters, Sub expression Elimination, Multiple Constant Multiplication, Sub expression Sharing in digital filters, Additive and Multiplicative Number splitting.	8
3	**Bit-Level Architecture** Parallel Multipliers, Interleaved Floor-Plan and Bit-Plane Based Digital Filters, Bit-Serial Multipliers, Bit Serial Filters Design and Implementation, Canonic signed Digit Arithmetic, Distributed Arithmetic.	6
4	**Redundant Arithmetic** Redundant Number Representations, Carry-Free Radix-2 Addition and Subtraction, Hybrid Radix-4 Addition, Radix-2 Hybrid Redundant Multiplication Architectures, Data format Conversion, Redundant to non redundant Converter	4
5	**Scaling and Round-off Noise** Scaling and Round-off Noise, State Variable Description of Digital Filters, Scaling and Round-off Noise computation, Round-off Noise in pipeline IIR Filters, Round-off Noise Computation Using State Variable Description, Slow-Down, Retiming and Pipeline.	6
6	**Pipelined and Parallel Recursive and Adaptive Filters** Pipeline Interleaving in Digital Filters, Pipelining in 1st Order IIR Digital Filters, Pipelining in Higher Order IIR Digital Filters, Parallel processing for IIR filters, Combined pipelining and parallel processing for IIR filters. Low power IIR filter design using pipelining and parallel processing, Pipelined Adaptive digital filters.	6

Text Book:

"VLSI digital signal processing systems- Design & Implementation" by Keshab Parhi, Wiley publication, Edition 2007 .

***Minimum 8 tutorials can be conducted based on the above syllabus**

M.E. (VLSI and Embedded Systems) Semester-II

Automotive Embedded Systems

Elective II

Lectures: 3 Hrs/week **Theory:** 100 marks
Tutorial: 1 Hr/week **Term Work:** 25 marks

Unit	Contents	Hrs
1	**Internal Combustion Engine Fundamentals** Engine types and their operations: Engine Operating Cycles, Engine Components, Spark-Ignition Engine Operation, Examples of Spark-Ignition Engines, Compression-Ignition Engine Operation, Engine parameters: Geometrical Properties of Reciprocating Engines, Brake Torque and Power, Indicated Work per Cycle, Mechanical Efficiency, Road-Load Power, Mean Effective Pressure, Specific Fuel Consumption and Efficiency, Air/Fuel and Fuel/Air Ratios, Thermo-chemistry of Air-fuel mixture: Ideal Gas Model, Composition of Air and Fuels, Combustion Stoichiometry	6
2	**Automotive Electronic Control Systems** Power train domain: Engine control unit, Electronic fuel injection control, Electronic ignition control, Chassis domain: ABS, ESP, EPS, Body domain: Doors, window lift, seat control, lighting, heating, ventilation and AC control, Automotive sensors and actuators required for above domains.	6
3	**Automotive Networks** Automotive communication system: characteristics and constrains, In-car embedded networks review, Middleware, AUTOSAR, Issues for automotive communication system, Study of automotive communication standards: CAN, Flex-Ray, review of LIN bus.	10
4	**Model Based Software Development** Product lines in automotive electronics, MBD for Automotive Embedded Systems, Context, Concerns, and Requirements, MBD Technology, State of the Art and Practice, Guidelines for Adopting MBD	6
5	**Testing Automotive Control Software** Test Activities and Testing Techniques, Testing in the Development Process Test Planning Testing and Monitoring of Flex-Ray Based Applications , Objectives for Testing and Monitoring, Monitoring and Testing Approaches Discussion of Approaches	6
6	**Timing Analysis of CAN-Based Automotive Communication Systems** CAN Schedulers, Scheduling Model, Response Time Analysis, Timing Analysis Incorporating Error Impacts, Holistic Analysis, middle-wares and Frame Packing	6

Text books:

- "Internal Combustion Engine Fundamentals", John B. L Heywood, Mc-GrawHill Inc.
- "Automotive Embedded Systems Handbook", edited by Nicolas Navet , CRC press

Reference books

- "Understanding Automotive Electronics", by Williams Ribbens, Elsevier Pub
- "Automotive Electronics Handboo", Ronald K. Jurgen McGrawHill Inc
- "BOSCH CAN Specifications Version 2".
- "FlexRay and its Applications", Dominique Pret, Wiley Publication

***Minimum 8 tutorials can be conducted based on the above syllabus.**

M.E. (VLSI and Embedded Systems) Semester-II

Low power VLSI Design

Elective II

Lectures: 3 Hrs/week **Theory:** 100 marks
Tutorial: 1Hr/week **Term Work:** 25 marks

Unit	Contents	Hrs
1	**Technology & Circuit Design Levels** Sources of dissipation in digital ICs, degree of freedom, recurring themes in low-power, emerging low power approaches, dynamic dissipation in CMOS, effects of V_{dd} & V_t on speed, constraints on V_t reduction, transistor sizing & optimal gate oxide thickness, impact of technology scaling, technology innovations	8
2	**Low Power Circuit Techniques** Power consumption in circuits, flip-flops & latches, logic, high capacitance nodes, energy recovery CMOS- example, some practical details, retractile logic, reversible pipelines, high performance approaches	6
3	**Low Power Clock Distribution** Power dissipation in clock distribution, single driver versus distributed buffers, buffers & device sizing under process variations, zero skew Vs. tolerable skew, chip & package co-design of clock network.	6
4	**Logic Synthesis for Low Power** Power estimation techniques, power minimization techniques, low power arithmetic components- circuit design styles, adders, multipliers, division.	8
5	**Low Power Memory Design** Sources & reduction of power dissipation in memory subsystem, sources of power dissipation in DRAM & SRAM, low power DRAM circuits, low power SRAM circuits	6
6	**Low Power Microprocessor Design** System power management support, architectural trade offs for power, choosing the supply voltage, low-power clocking, implementation problem for low power, comparison of microprocessors for power & performance.	8

Text Book:

"Low Power Design Methodologies", P. Rashinkar, Paterson and L. Singh, Kluwer Academic, 2002

Reference Books:

"Low power CMOS VLSI circuit design", Kaushik Roy, Sharat Prasad, ISBN: 0-471-11488-x, John Wiley & sons Inc.

***Minimum 8 tutorials can be conducted based on the above syllabus**

M.E. (VLSI and Embedded Systems) Semester-II

System on Chip Architecture-II

Elective II

Lectures: 3 Hrs/week **Theory:** 100 marks
Tutorial: 1Hr/week **Term Work:** 25 marks

Unit	Contents	Hrs
1	**Custom Bus-Based On-Chip Communication Architecture Design** Split Bus Architectures, Serial Bus Architectures, CDMA-Based Bus Architectures, Asynchronous Bus Architectures, Dynamically Reconfigurable Bus Architectures.	6
2	**On-Chip Communication Architecture Refinement and Interface Synthesis** On-Chip Communication Architecture Refinement, Interface Synthesis, Discussion: Interface Synthesis	6
3	**Verification and Security Issues in On-Chip Communication Architecture Design** Verification of On-Chip Communication Protocols, Compliance Verification for IP Block Integration, Basic Concepts of SoC Security, Security Support in Standard Bus Protocols, Communication Architecture Enhancements for Improving SoC Security	6
4	**Physical Design Trends for Interconnects** DSM Interconnect Design , Low Power, High Speed Circuit Design Techniques, Global Power Distribution Networks, Clock Distribution Networks, 3-D Interconnects	6
5	**Networks-On-Chip** Network Topology, Switching Strategies, Routing Algorithms, Flow Control, Clocking Schemes, Quality of Service, NoC Architectures, NoC Status and Open Problems	8
6	**Emerging On-Chip Interconnect Technologies** Optical Interconnects, RF/Wireless Interconnects, CNT Interconnects	4

Text Book:

"On-Chip Communication Architectures: System on Chip Interconnect", Sudeep Pasricha and Nikil Dutt, Morgan Kaufmann Publishers © 2008

Reference Books:

- "Transaction Level Modeling with SystemC: TLM Concepts and Applications for Embedded Systems", Frank Ghenassia, Springer © 2005 (281 pages), ISBN:9780387262321
- "Networks on Chips: Technology and Tools", Luca Benini and Giovanni De Micheli, Morgan Kaufmann Publishers © 2006 (408 pages), ISBN:9780123705211

***Minimum 8 tutorials can be conducted based on the above syllabus**